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MUNDFAB

Modeling Unconventional Nanoscaled Device FABrication

D6.1: Device architectures and processing of the test applications

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Abstract

This deliverable describes the device architectures and process steps of the test applications that will be used to evaluate and validate the models developed in the MUNDFAB project (WPs 2 to 5).

1 FDSOI devices

In the frame of the MUNDFAB project, CEA will provide test applications based on FDSOI technology processed with a low thermal budget which can be integrated in a 3D sequential integration scheme. Two junction strategies are considered (see [1,2]):

- The XLast integration, where the junction is defined after the formation of offset spacers
- The XFirst integration, where dopants are located close to the gate through a thin liner before the offset spacer formation.

The full transistor process for each strategy will be described in the following sections. It should be noted that the devices are MOSFETs with gate lengths down to 30 nm.

1.1 XLast integration

The XLast general process flow is presented in Fig. 1 for two different device geometries, TriGate and planar. The two geometries essentially differ in the film thickness and the width (W) of the active region. In the case of planar devices, the substrate is a Silicon on Insulator (SOI) with a film and BOX thickness of 7 and 145 nm, respectively and a nominal W of 0.21 µm. In contrast, TriGate devices have a smaller W down to 15 nm and a film thickness of 11 nm. TEM cross sections of TriGate devices are shown in Fig. 2 and Fig. 3.

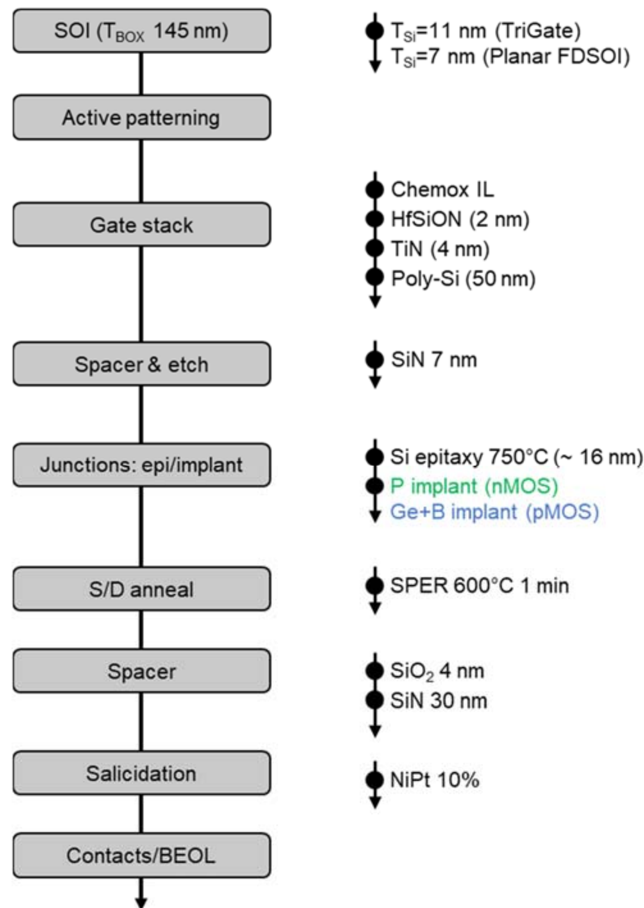

Fig. 1: Low thermal budget process flow of an XLast integration. nMOS and pMOS variations are given in green and blue, respectively.

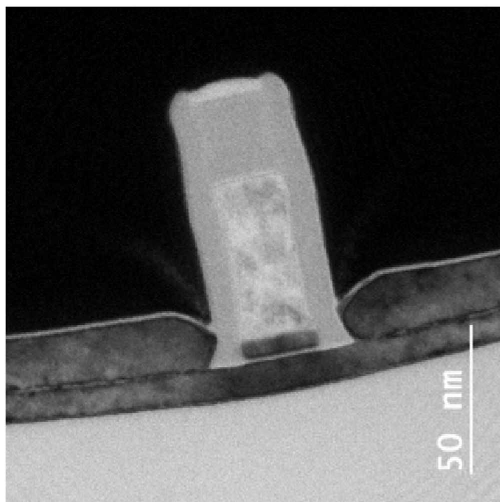

Fig. 2: TEM cross section of low temperature TriGate device.

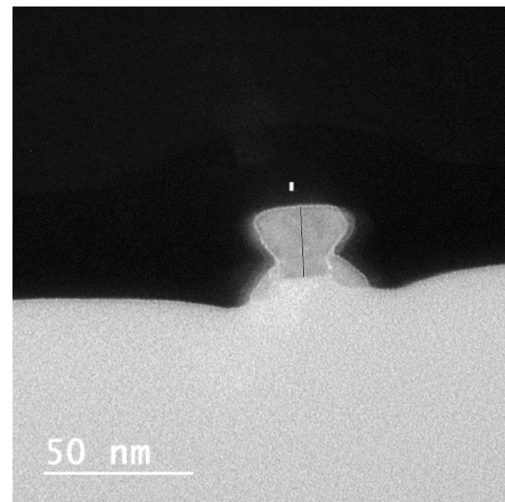

Fig. 3: TEM cross section in lateral direction of low temperature TriGate device.

In this integration, junction formation involves an amorphization of the crystalline substrate using ion implantation, either with the dopant itself or using a pre-amorphization implantation (PAI) with heavier species such as Ge. Then, the amorphized region re-crystallizes through Solid Phase Epitaxial Regrowth (SPER) performed with a low thermal budget (typically below 600 °C), allowing dopants to be activated.

1.2 XFirst integration

In the case of an XFirst integration, only planar devices have been fabricated. The substrate is an SOI with a Silicon film and BOX thickness of 6 nm and 20 nm, respectively. In the case of the pMOS, the channel is enriched in Ge (SiGe 27%) with the same thickness. The complete process flow is shown in Fig. 4.

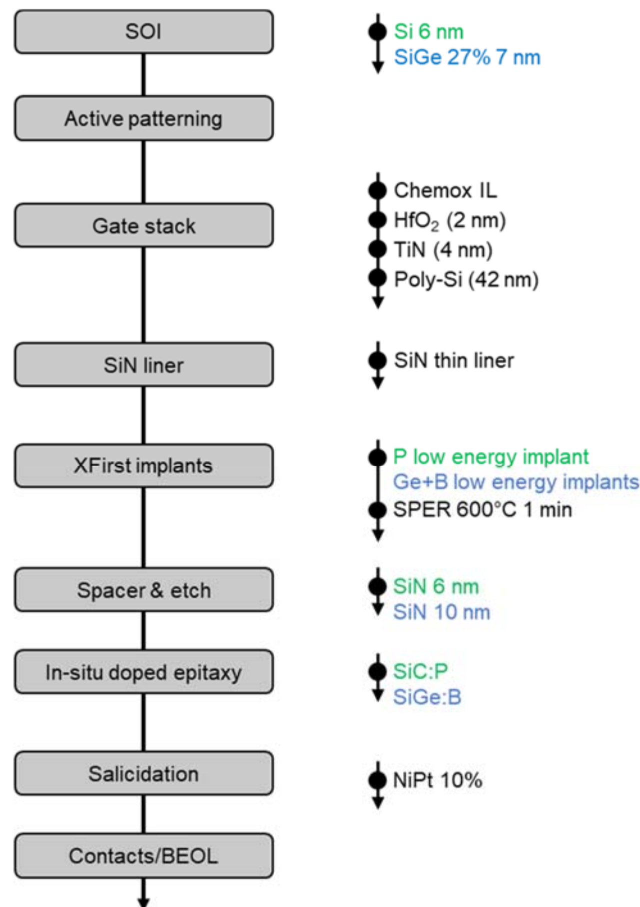

Fig. 4: Low thermal budget process flow of an XFirst integration. nMOS and pMOS variations are given in green and blue, respectively.

Compared to an XLast integration, the main differences are related to the junction process, described in detail in Fig. 5. Finally, TEM cross-sections of nMOS and pMOS devices are shown in Fig. 6.

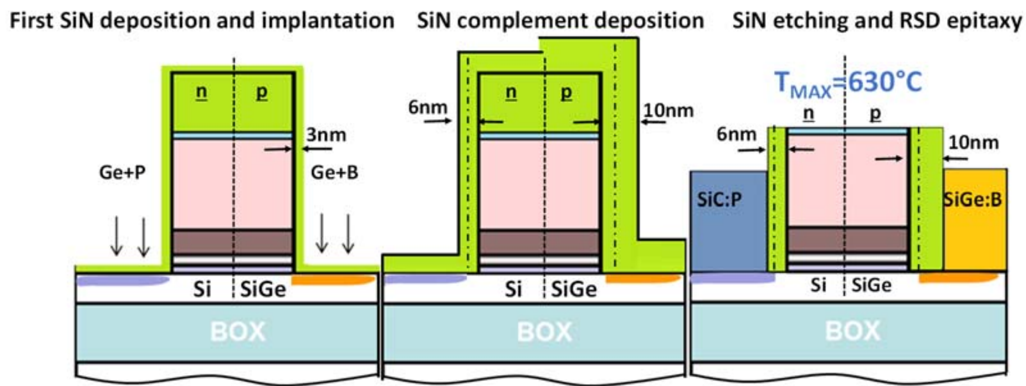

Fig. 5: Junction formation process in an XFirst integration for nMOS (left) and pMOS (right)

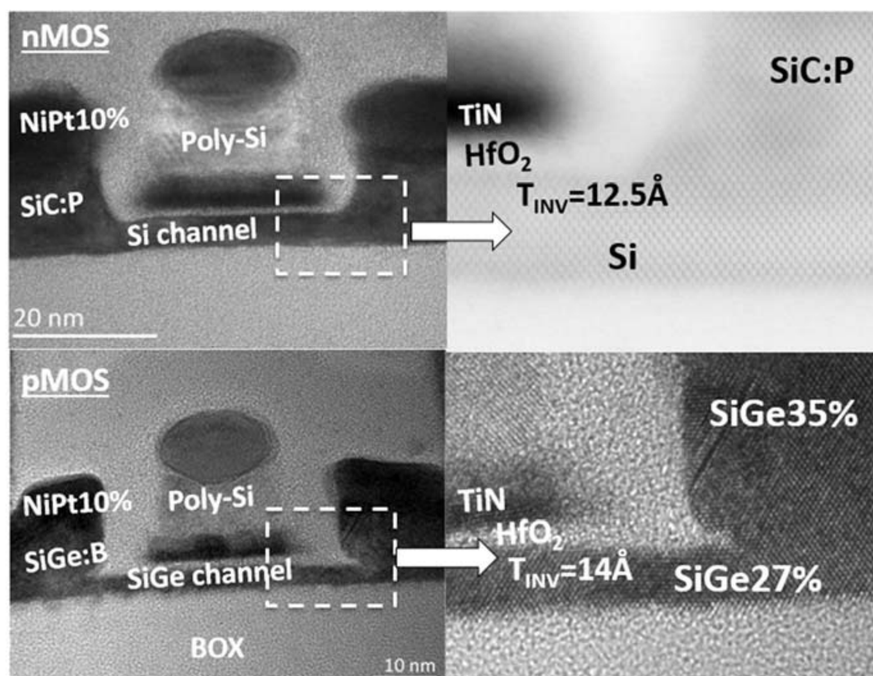

Fig. 6: TEM cross-sections of nMOS and pMOS fabricated with an XFirst process flow

2 Vertical GAA NW-FETs with silicided source/drain contacts

In the frame of the MUNDFAB project, LAAS-CNRS will provide test applications based on Vertical Gate-All-Around (GAA) transistor technology with source/drain contacts fabricated at temperatures below 400°C. The proposed architecture is a Vertical Field Effect Transistor (VFET) implemented on a Si NW array with three contacts vertically stacked and connected to extrinsic access points thanks to vias and metallization [3, 4]. A common gate-all-around surrounds each conductive NW to get parallel channels within a single transistor. Symmetric metallic S/D contacts connect the uniformly highly doped nanowires. The complete process flow is shown in Fig. 7.

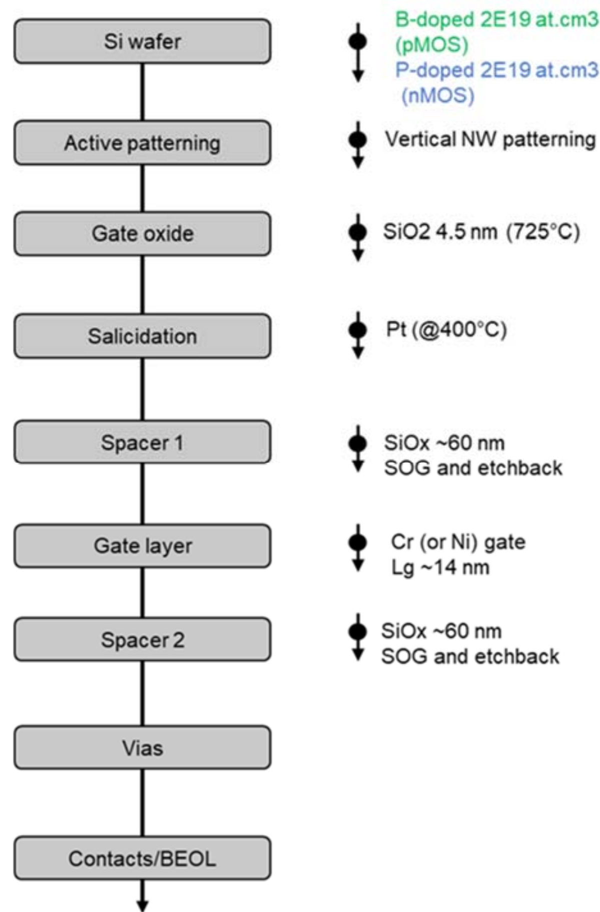

Fig. 7: Process flow of vertical GAA transistor with nanoscale gate lengths where pMOS and nMOS variations are given in green and blue, respectively.

Fig. 8 is a TEM cross-section of the final device demonstrating the possibility of integrating massively parallel dense NW arrays with symmetrically silicided S/D contacts and scaled metallic gate-all-around (Lg ~ 14 nm) architecture [3].

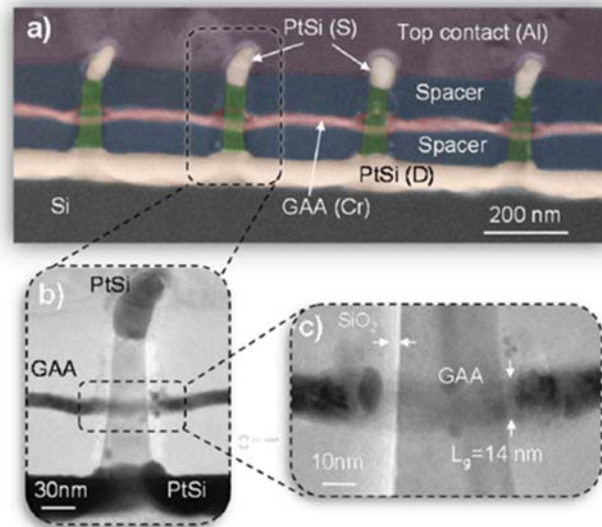

Fig. 8: Transmission electron micrographs of the vertical nanowire array transistor. (a) TEM cross section in tilted view with false color of the device with a gate surrounding each nanowire, symmetrically silicided S/D (PtSi) contacts and 70 nm low k (2.7) dielectric spacers separating the S/D contacts from the gate, (b) a zoom of the TEM cross section with a nice planarity of the stacked layers and (c) a zoom of the GAA region with the 5 nm SiO_2 gate oxide and the 14 nm gate length (from [3]).

Conclusions

Test applications have been presented and can be implemented in TCAD decks in order to simulate the different process steps involved in the fabrication of real devices. They will allow to validate the models developed in the MUNDFAB project (WPs 2 to 5) including:

- Dopant activation using SPER at temperatures below 600 °C (WP2)
- Morphology of Raised Source/Drain regions after CVD epitaxy (WP3)
- Dopant activation during CVD epitaxy (WP3)
- Silicidation (WP2)
- Post-anneals (WPs 2 and 3)
- Gate oxide reliability (WP5)

So far, heated implants and ns laser anneals have not been integrated in the fabrication of real devices. Therefore, they are not part of the process flows corresponding to the test applications described in this deliverable.

References

[1] L. Pasini *et al.*, VLSI Technology (2015)
[2] L. Pasini *et al.*, VLSI Technology (2016)
[3] G. Larrieu, X.L. Han, Nanoscale, 5, (2013) 2437–2441
[4] Y. Guerfi, G. Larrieu, Nanoscale research letters, 11 (2016) 210