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MUNDFAB

Modeling Unconventional Nanoscaled Device FABrication

D6.3: Report on the toolchains for the test applications

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Contents

1 Executive Summary

This document describes the simulation toolchains developed for the test applications described in the MUNDFAB deliverable D6.1. The toolchains include the modeling results from work packages (WP) 2 to 5. Some of these novel modeling advancements are embedded in in-house external simulation tools, which provide improved capabilities with respect to conventional commercial Technology Computer Aided Design (TCAD) tools. However, the employed external tools can address only specific process steps, so to simulate a full process flow they must be integrated into the flow of standard TCAD tools (Synopsys Sentaurus in this case). The simulation toolchains presented in this deliverable employ both standard Synopsys Sentaurus TCAD tools and external simulators and they are based on the integration strategies described in D6.2. In D6.2, a coupling procedure to interface the external super-Lattice Kinetic Monte Carlo (KMCsL) tool `MulSKIPS` [1], used in WPs 2 to 4, and Synopsys Sentaurus TCAD tools was reported. D6.2 also describes an integration strategy between Synopsys TCAD and the external off-lattice kinetic Monte Carlo method and density functional theory (DFT) calculations developed in WP5.

Four different demonstrators, three for the test applications presented in D6.1 and an additional one, are reported in this deliverable. The first demonstrator presented is based on Fully Depleted Silicon On Insulator (FDSOI) devices fabricated following the XLast integration (see D6.1 for more details). A planar and a trigate MOSFETs are addressed, sharing the same process flow, except for the active area patterning before gate stack formation. The simulation toolchain integrates `MulSKIPS` for the simulation of raised source/drain epitaxial growth. After, the process simulation continues in Sentaurus Process with an amorphizing implantation and subsequent Solid Phase Epitaxial Regrowth (SPER). The second demonstrator is a planar FDSOI device fabricated following the XFirst integration (see D6.1). In this case, the raised sources/drains are fabricated by an *in-situ* doped epitaxial growth performed after an implantation step. The process simulation toolchain does not include `MulSKIPS` for the simulation of epitaxial deposition steps because of the presence of dopants. `MulSKIPS`' resource-intensive super-lattice framework (involving both cubic and hexagonal stacking configurations, more details can be found in D3.4 and [2]) is not computationally efficient in this case, due to the relative low probability of the dopant incorporation events (about 1%). Plus, the dopant diffusion cannot be simulated. The full process toolchain is implemented in Sentaurus Process. Sentaurus Process' standard cubic LKMC framework, in fact, allows for usage of larger simulation cells, which improves statistics for dopant incorporation events. Moreover, contrary to `MulSKIPS`, Sentaurus Process' LKMC epitaxy module is coupled to the KMC module for dopant diffusion and activation. The last demonstrator from D6.1 is a Vertical Gate-All-Around (GAA) nanowire (NW) field-effect transistor (FET). For this demonstrator, the process simulation toolchain includes `MulSKIPS` for the simulation of silicidation. All the simulation toolchains of these demonstrators can integrate the results of WP5 on device reliability in the final device simulations. A fourth additional demonstrator, not described in D6.1, is also presented here. It consists of a silicon germanium nanowire on top of a strained silicon germanium layer on a silicon substrate, which undergoes a nanosecond pulsed laser annealing (LA) process. This test application demonstrates the possibility of integrating `MulSKIPS` LA simulations, developed in WP4, within the Synopsys tools.

The evaluation of the novel simulation toolchains reported here, against standard modeling approaches and experimental data, will be presented in D6.4. As the process simulation toolchains for the FET devices are coupled to device simulations, electrical measurements can

be used for the model's evaluation. Finally, the user's feedback about the toolchains will be reported in D6.5.

2 FDSOI demonstrator – XLast integration

The first test application described in D6.1 is the FDSOI MOSFET, in planar or TriGate device geometry, with XLast integration, fabricated at CEA-Leti. Figure 2.1, adapted from D6.1, describes the process flow for the fabrication of the transistors. It also reports a schematic summary of the process simulation toolchain used to simulate the process steps. In particular, for this demonstrator, the epitaxy is simulated using the external KMCsL tool `MulSKIPS` [1, 3], which includes the novel modeling advancements for epitaxial growth developed in WP3, which were preliminarily described in D3.4 and will be reported in their final version in D3.6. A consistent simulation toolchain for the full process flow is obtained thanks to the coupling strategy (from Synopsys to `MulSKIPS` and from `MulSKIPS` to Synopsys) previously developed and described in D6.2. The full simulation toolchain runs in Synopsys Sentaurus Workbench [4] platform. The workbench project, as shown in Figure 2.2, embeds both the internal Synopsys Sentaurus tools (Sentaurus Process [5], Structure Editor [6], Data Explorer [7], Device [8] and Visual), and the external tools used for the atomistic simulations

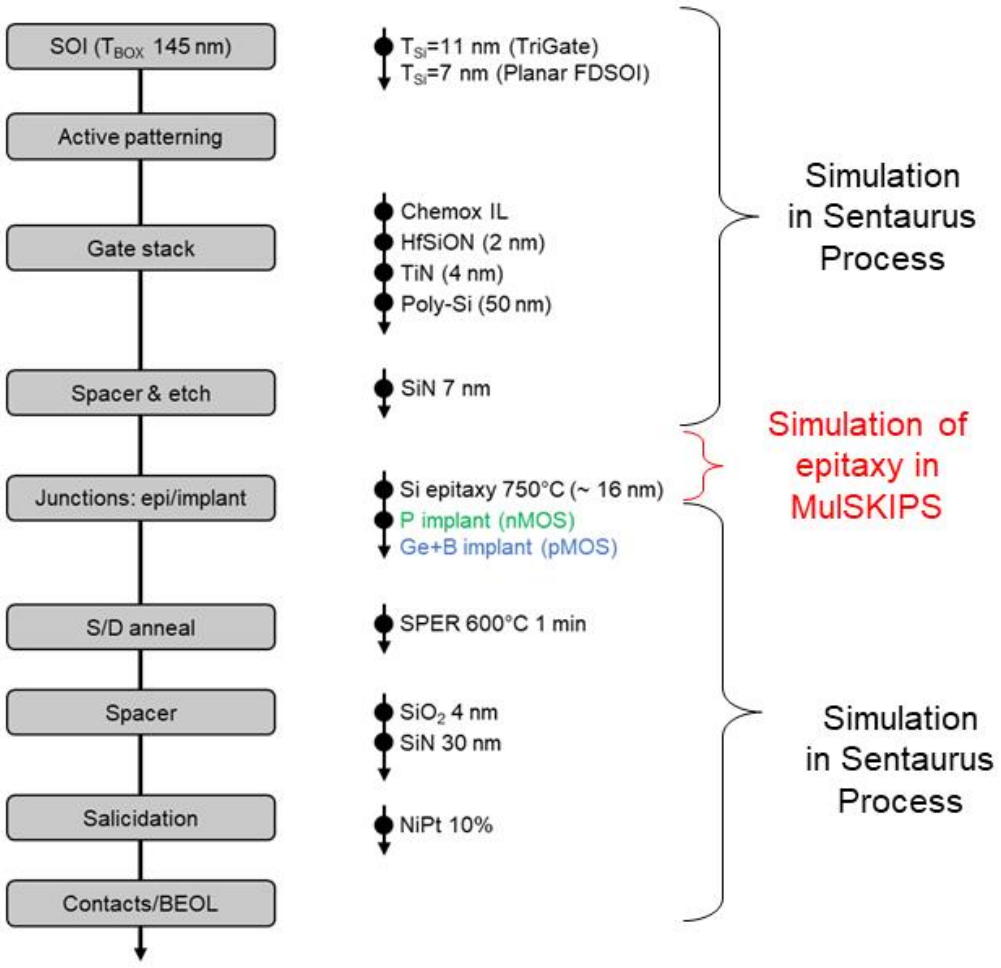


Figure 2.1 – Fabrication process flow for FDSOI transistors in the XLast integration (see D6.1) and corresponding simulation tool used for the modeling.

	type	L				MSKIPS_ITERMAX	MinZSurf			Temperature Anneal		mesh	Vbg	Vdd	Vgg	
1	nmos	5	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
2		10	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
3		20	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
4		30	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
5	pmos	5	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
6		10	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
7		20	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--
8		30	--	--	--	450e6	0.022	--	--	600	--	1	0.0	0.8	0.8	--

Figure 2.2 – Screenshot of the of the full simulation toolchain captured from the Sentaurus Workbench project. The toolchain includes internal Sentaurus tools (Process, Data Explorer, Structure Editor, Device, Visual), external tools (`MulSKIPS`, `DEP3D`) and Python scripts.

(`MulSKIPS` [1]) and for the coupling procedure (`DEP3D` [9] and various Python scripts). In this way, the full simulation toolchain can be run smoothly within a common frame.

2.1 Planar geometry

The simulation toolchain of this test application starts within the Synopsys TCAD environment. Firstly, the FDSOI substrate is defined in Sentaurus Process [5]. Then, the deposition and patterning of the gate stack is simulated. A gate length of 40 nm is considered here. After, the SiN spacer 0 is included. The structure obtained after this step is shown in Figure 2.3. The next step in the process flow is the silicon epitaxy to grow the raised source and drain. In the XLast integration scheme, the epitaxy is undoped and the implantation for junction formation is performed after the epitaxy. The epitaxial growth is simulated in `MulSKIPS` starting from the structure created in Sentaurus Process, therefore the coupling procedure to interface `MulSKIPS` and Synopsys Sentaurus Process, described in D6.2, is applied. Thanks to the bi-directional coupling procedure, it is then possible to simulate the subsequent implantation with Sentaurus Process on the raised source and drain geometry as simulated by `MulSKIPS`. Starting from the 2D structure in Sentaurus Process, shown in Figure 2.3, a 3D structure needs to be generated for a correct simulation in `MulSKIPS`. For this reason, an extrusion of 5 nm is performed in Sentaurus Process, followed by a reflection with respect to the gate stack axis, to obtain the final structure with the gate stack in the middle. This is needed since `MulSKIPS` employs periodic boundary condition for the KMCsL box, so it is necessary to have the same material, i.e. silicon, at the two edges of the simulation box. The structure is also cut under the BOX to reduce computational cost in `MulSKIPS` simulations. The latter, visualized with Sentaurus Visual, is shown in Figure 2.4. At this point, the structure is still in TDR Synopsys format (see D6.2 for a detailed explanation of file formats). Following the coupling procedure, the structure is exported in GRD format using Sentaurus Data Explorer and then converted in MSH format. The structure in MSH format is shown in Figure 2.5, as visualized with `gmsh` [10], [11]. Further conversion steps are performed in `pyMulSKIPS`, i.e., the Python interface of `MulSKIPS`, to enable reading of the MSH-formatted geometry in `MulSKIPS`.

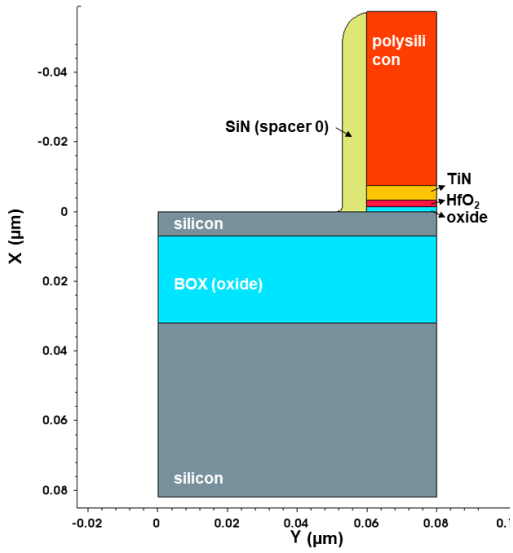


Figure 2.3 - FDSOI substrate with gate stack, simulated in Sentaurus Process.

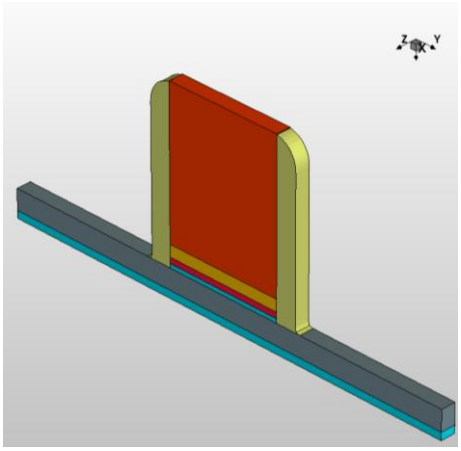


Figure 2.4 – Extruded 3D structure in Sentaurus environment before the import in the MulSKIPS environment during the coupling procedure.

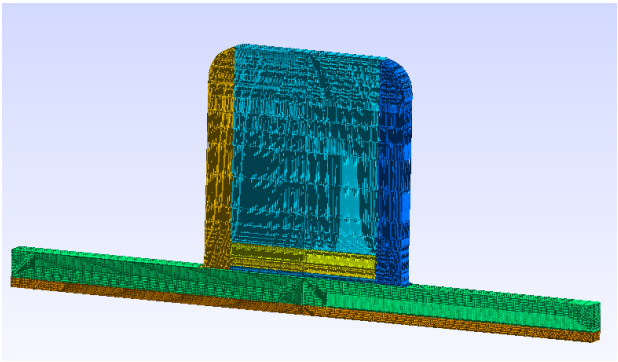


Figure 2.5 - Structure from Figure 2.4 converted in MSH format, readable by MulSKIPS. The MSH file is visualized in gmsh [10], [11].

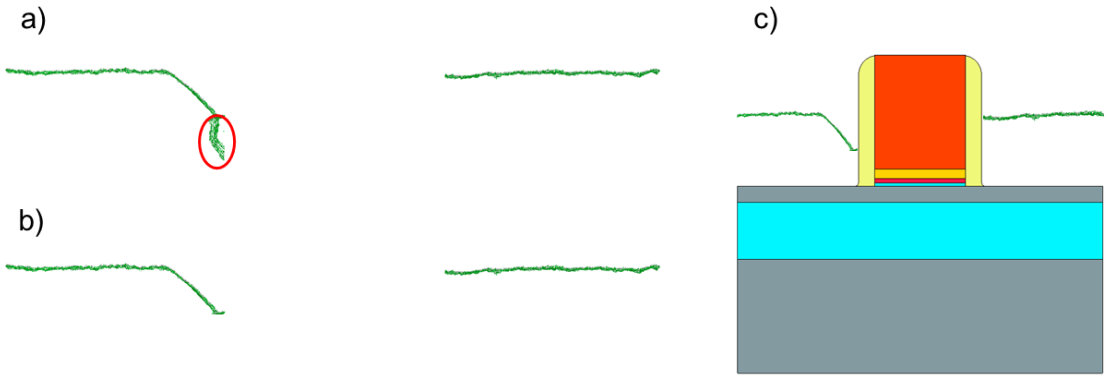


Figure 2.6 – a) Output of MulSKIPS simulation used for the coupling procedure from MulSKIPS back to Synopsys Sentaurus: surface atoms (silicon and coverage atoms H and Cl) describing the solid-gas interface and consequently the new surface of the structure after the KMCsL simulation. Stacking faults in contact with the gate stack are highlighted in red circles. b) Surface nodes after the elimination of the stacking fault: these can be correctly handled by DEP3D in the MulSKIPS to Sentaurus coupling procedure. c) Surface nodes superimposed to the FDSOI structure captured before epitaxy simulation.

Then, the MulSKIPS simulation can be finally run. In this case, a well calibrated MulSKIPS KMCsL simulation of Si CVD growth with SiH_2Cl_2, HCl and H_2 precursors is carried out. The output needed for the import of the simulated geometry into the Synopsys Sentaurus environment is a file containing the coordinates of the surface atoms (the silicon surface atoms and the coverage atoms, H and Cl), which determine the solid-gas interface and so the new surface of the structure after the KMCsL simulation. The surface atoms are shown in Figure 2.6.a. We note that the facet formation close to the stack is a stochastic phenomenon in MulSKIPS, which depends on input parameters such as the periodic cell dimensions or the probability of breaking the ideal cubic stacking. To highlight the effect of faceting on the post-epitaxy implantation results, we chose to set up the simulation as to yield faceting on one side only. The red circle highlights defects (stacking faults) that originate from being in contact with the gate stack (see Figure 19 in D3.4 for further details). These defects cannot be handled in the subsequent coupling procedure (from MulSKIPS to Synopsys Sentaurus) and are therefore eliminated by a post-processing script, obtaining the surface nodes as reported in Figure 2.6.b. Figure 2.6.c features the surface atoms superimposed to the initial FDSOI structure before MulSKIPS simulations, showing how the raised source/drain geometry

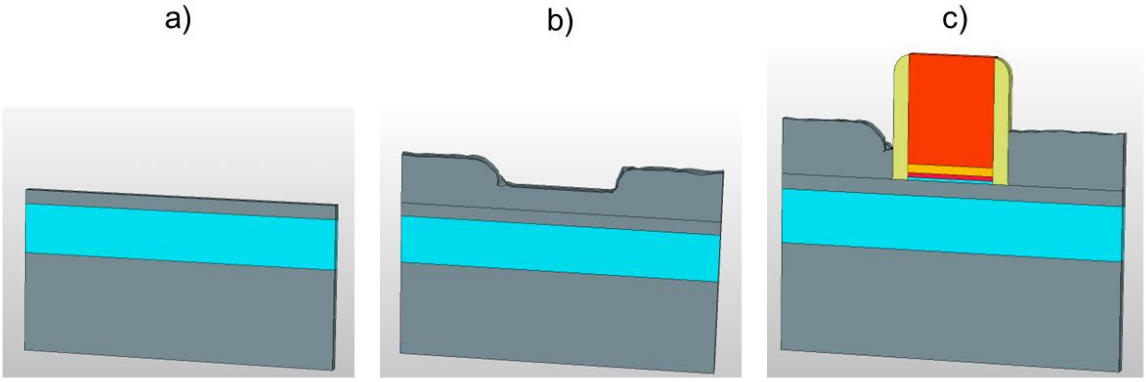


Figure 2.7 – a) Input structure used by DEP3D: gate stack removed. b) Output structure of DEP3D, using as inputs the surface nodes in Figure 2.6.b and the structure in a). c) With a Boolean operation, the gate stack is reintroduced and the final structure including the result of simulated epitaxial growth is obtained.

should look like. The coupling procedure from MulSKIPS back to Synopsys Sentaurus follows the one described in D6.2, with a slight difference. The deposition simulator DEP3D determines a polyhedron describing the new topography entity with a triangle-based description, based on the surface nodes provided by MulSKIPS, as in D6.2. However, in this case, DEP3D does not use the full structure before MulSKIPS simulation (Figure 2.4), but the structure without the gate stack (Figure 2.7.a). This is done because DEP3D can only construct a continuous new region covering the entire structure surface, without interruption. The output structure, including the grown silicon described with a polyhedron, is shown in Figure 2.7.b. Finally, thanks to a Boolean operation with the original structure before epitaxy with gate stack (Figure 2.4), the final structure with correct geometry is obtained, as shown in Figure 2.7.c. The last step of the coupling procedure consists in a remeshing of the structure, which is then ready for the simulation of the next process step in Synopsys Sentaurus Process. The structure can be kept in 3D or it can be transformed back to a 2D structure as before the MulSKIPS simulation. For the subsequent steps we choose to go back to a 2D structure. To do so, a slice from the 3D structure is cut using Sentaurus Structure Editor (there is no break of symmetry in the direction of the extrusion, so a simple cut is sufficient). The final steps of the process flow are simulated in Sentaurus Process, as shown in the screenshot of the Workbench project in Figure 2.2 (on the right of Sentaurus Structure Editor SDE). The implantation (Figure 2.8.a) and annealing (Figure 2.8.b) steps are simulated using the atomistic KMC simulation framework of Sentaurus Process. The figures are in 3D because the KMC framework of Sentaurus Process automatically extrudes a 2D structure into a 3D one. A conversion back to continuum simulations is then performed. For a better convergence in device simulations, a smoothing step is necessary. The Sano method [12] is therefore used to convert from KMC particles to appropriate finite element fields. The resulting structure is shown in Figure 2.9. As it can be noted, the different geometries of the raised source/drain regions (left and right of the gate stack) obtained from the simulation of epitaxial growth in MulSKIPS affect the resulting doping distribution after implantation and annealing simulation. This confirms the need of an accurate modeling of the epitaxial layer geometry. Next, a second spacer is added. Finally, the silicidation step is emulated by an etching of silicon and a subsequent deposition of silicide. The silicide regions are then “substituted” by the electrode regions (source/drain), i.e., the silicide is removed, and electrical boundary conditions are applied at the interface between silicide and silicon. Contacts at the bulk (bottom of the structure) and at the gate (both directly on top of the gate oxide and on top of the polysilicon region) are also placed, as depicted in

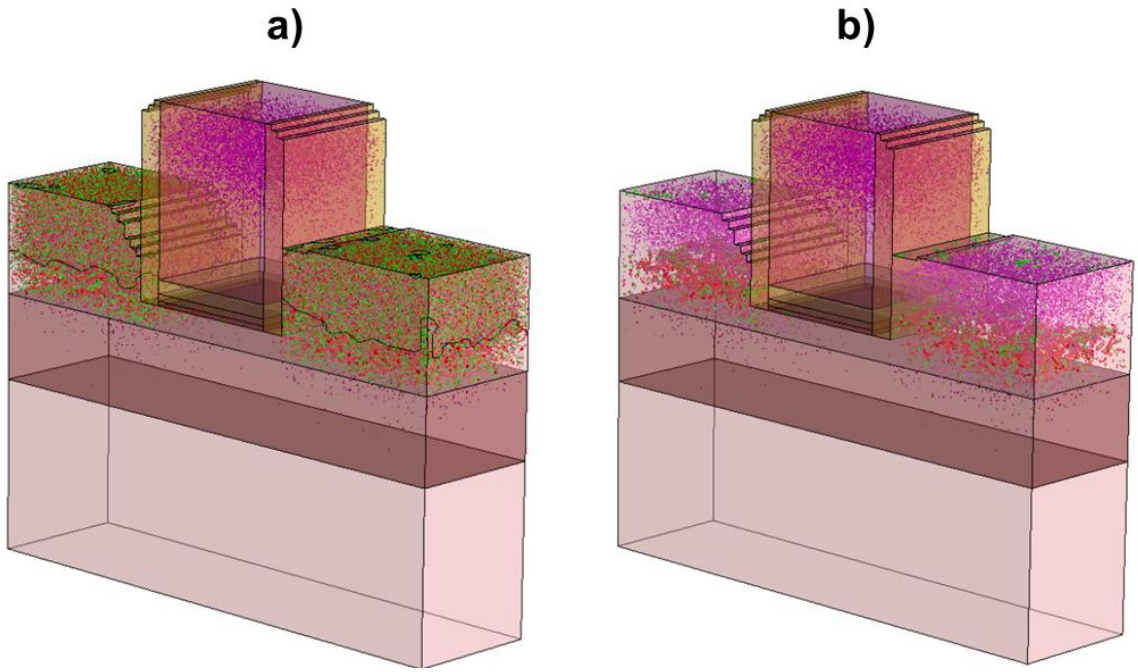


Figure 2.8 – a) Results of KMC atomistic simulation of implantation in raised source/drain regions; b) results of KMC simulation of annealing step after implantation. In a) and b) the coloured spheres represent the implanted dopants (phosphorous in this case, in magenta) and the damages in the crystals, such as vacancies, interstitials, clusters (silicon vacancies in green, silicon interstitials in red).

Figure 2.10, where electrical contacts are colored in magenta. This is to avoid convergence problems that can arise from the presence of too many metal/semiconductor interfaces in the gate stack. After remeshing, the final structure after process simulation (Figure 2.10) is used for device simulations. Device simulations are run in Sentaurus Device. The simulated transfer

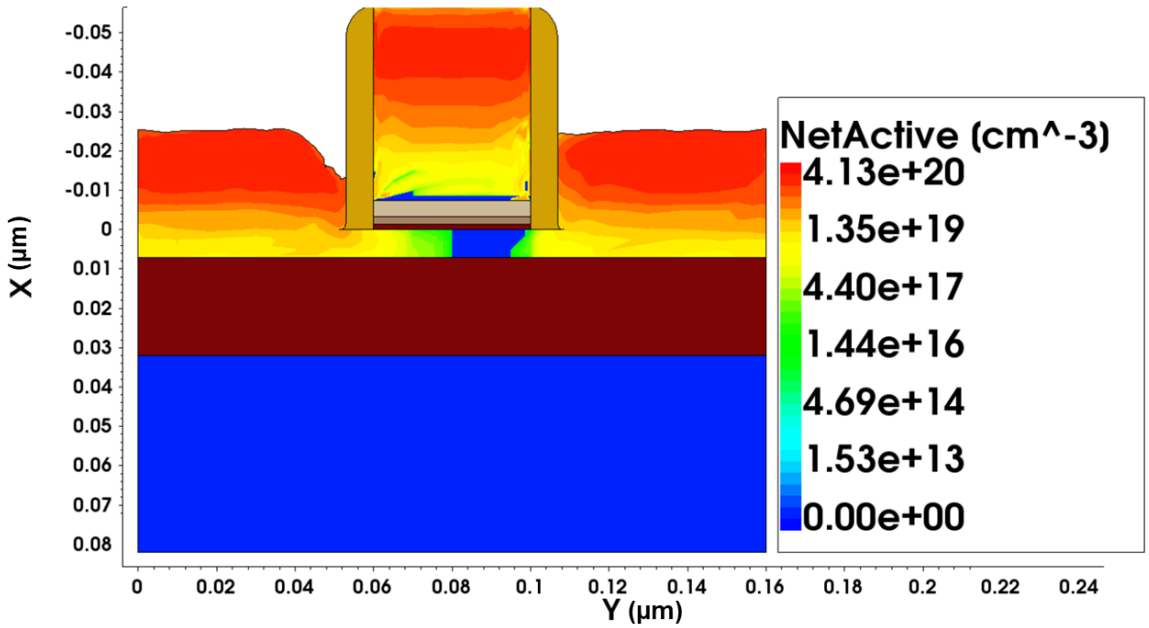


Figure 2.9 – Doping concentration (electrically active) from Sano method smoothing, used to convert KMC particles to appropriate finite element field.

characteristic, for a drain voltage of 0.8 V, is shown in Figure 2.11. Although the transfer characteristic does not show an ideal transistor-like behavior, as the simulated process conditions are not the optimal ones, these results show that the full simulation toolchain works correctly.

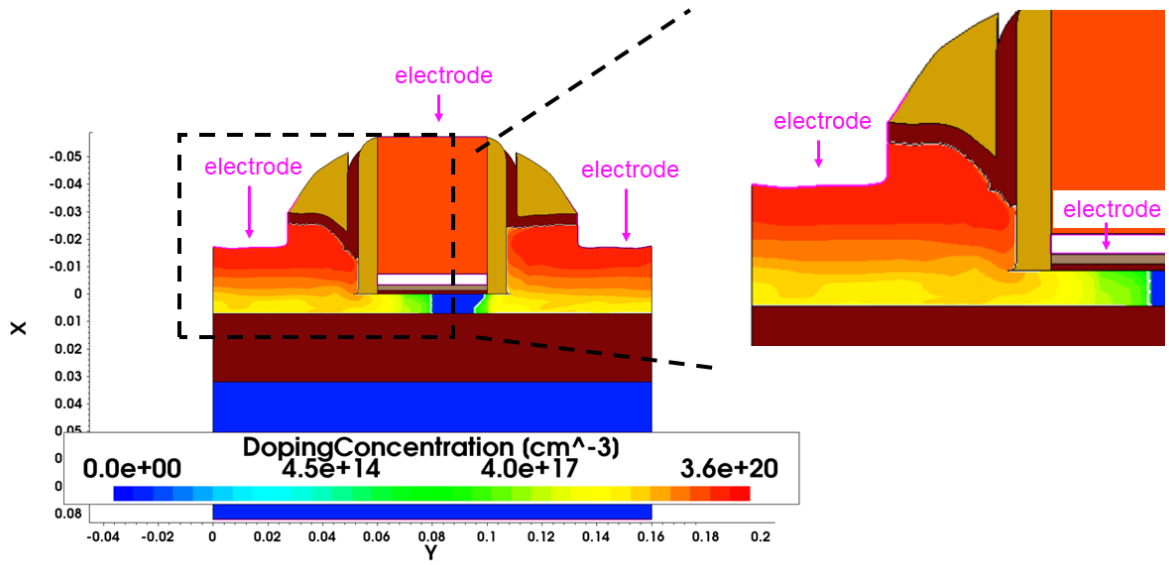


Figure 2.10 – Final structure used for device simulations. Contacts, where electrical boundary conditions are applied, are shown in magenta. A zoom in the source/gate region is shown for a better visualization of the contacts.

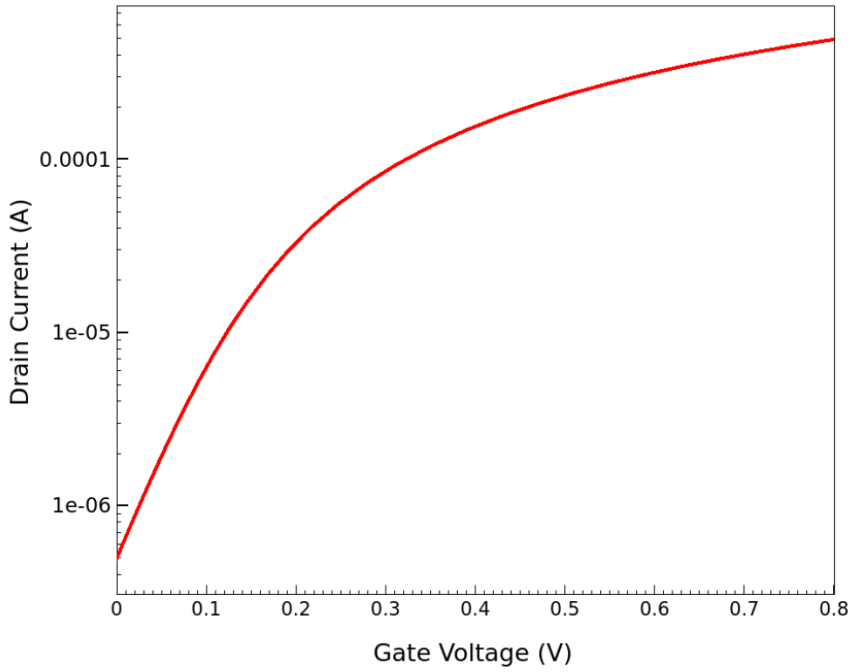


Figure 2.11 – Simulated transfer characteristics for the structure in Figure 2.10 (drain voltage = 0.8 V).

2.2 TriGate geometry

The transistors with XLast integration are also fabricated in TriGate device geometry. The process flow is the same as for the planar one, except for an active-area patterning. The simulation toolchain is also largely similar (see Figure 2.2). The only difference is that, unlike for the planar case, the structure is always simulated in 3D. Consequently, no extrusions of cut planes are needed here to convert from 2D to 3D and *vice versa*. The structure obtained in Sentaurus Process before the mirroring and the epitaxy simulation in `MulSKIPS` is shown in Figure 2.12. The integration strategy and `MulSKIPS` simulations follow the same procedure presented in the previous section. Figure 2.13 shows the device after `MulSKIPS` atomistic simulation of epitaxial growth, as imported back into the Synopsys environment. The simulation toolchain then continues in Sentaurus Process. The structure after KMC simulations of implantation and annealing is shown in Figure 2.14. The subsequent steps, as described above are also simulated and the toolchain ends with Sentaurus Device simulations. The simulated transfer characteristic is shown in Figure 2.15.

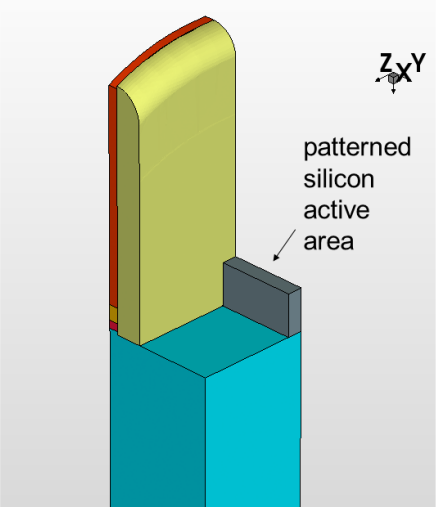


Figure 2.12 – TriGate structure obtained in Sentaurus Process, before the coupling procedure for the import in the `MulSKIPS` environment.

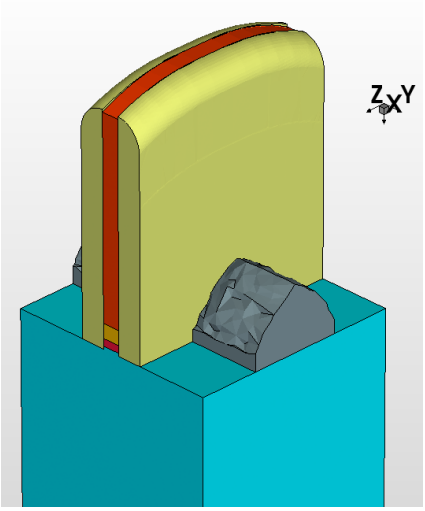


Figure 2.13 – TriGate structure after `MulSKIPS` simulations of epitaxial growth, as imported back in Synopsys environment.

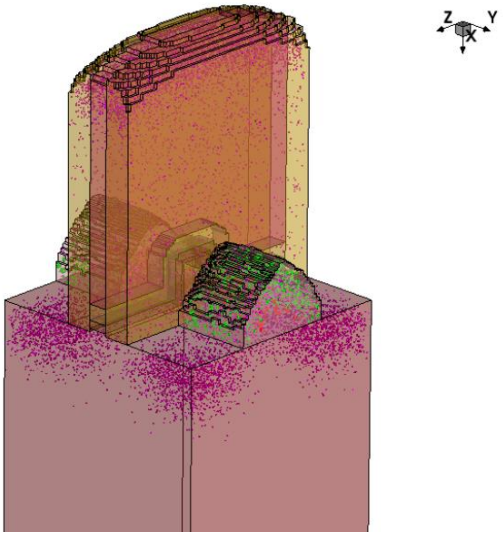


Figure 2.14 – TriGate structure after Sentaurus Process KMC simulations of implantation and anneal.

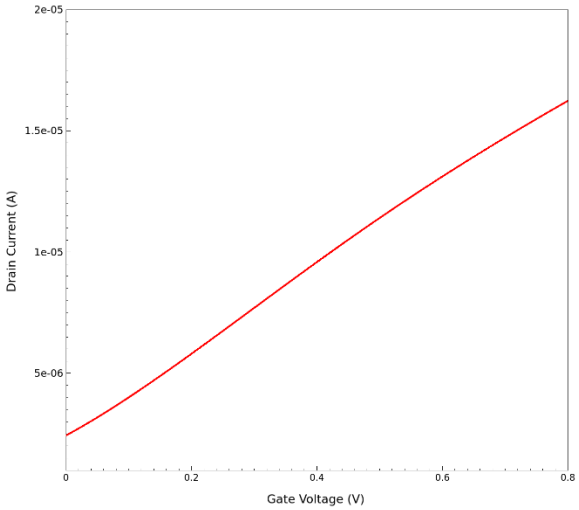


Figure 2.15 – Transfer characteristics simulated in Sentaurus Device at the end of the simulation toolchain.

2.3 Device reliability

In order to facilitate the various insights on device reliability gained within WP5, a link to Sentaurus Device has to be established. One key aspect of WP5 is the atomistic simulation of the thermal oxidation process of silicon and the evaluation of charge trapping parameters of oxide defects both from DFT modelling (see D5.2 and D5.4) and from experimental extraction, using electrical device characterization techniques (see D5.1 and D5.4). When it comes to describing the degradation of gate oxides, several different models with varying degrees of complexity/accuracy are currently used in industry, ranging from empirical power-law fits [13] to highly sophisticated physical models like the 4-state nonradiative multi-phonon (NMP) model [14] or the gate-sided hydrogen release model [15], see Figure 2.16.a. The 4-state NMP model, also often referred to as the extended NMP (eNMP) model, assumes two different charge states of the defect, with 2 additional metastable states (1', 2'), see Figure 2.16.b, in order to describe phenomena like anomalous random telegraph noise [16] or switching oxide traps [17]. While eNMP is typically employed to describe oxide degradation in TCAD software due to its versatility, its proper parametrization requires extensive experimental studies including labor-intensive single-defect characterization techniques like time-dependent defect spectroscopy (TDDS) [18]. In order to mitigate this, we absorb the metastable defect states into an effective 2-state model as shown in Figure 2.16.c, which can be parametrized easily from standard electrical device characterizations using the Comphy framework [19] developed at TU Wien.

Although the reduction to an effective 2-state model seems quite rough at first sight, it turns out that most of the physics is preserved relative to the eNMP model. This is particularly true for situations, where the device degradation is determined by a whole ensemble of defects instead of a few individual defects. Figure 2.17 shows a simulated comparison of the ΔV_{th} degradation between an effective 2-state and the extended 4-state model. As can be seen, the overall trend of the degradation is very well preserved in the simplified 2-state approach.

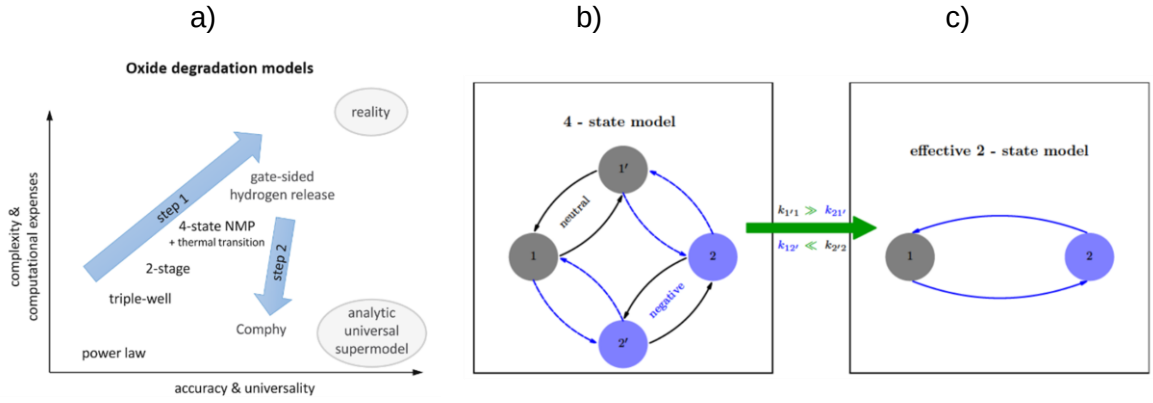


Figure 2.16 - Hierarchy of oxide degradation models with varying complexity and accuracy (a). The typically used 4-state NMP model (b) is very accurate, but difficult to parametrize properly from experimental data. Within the Comphy framework, the 4-state model is reduced to an effective 2-state NMP model (c), which is much simpler to compute and to parametrize using standard device characterization techniques. Figures are reproduced from [23] and [24].

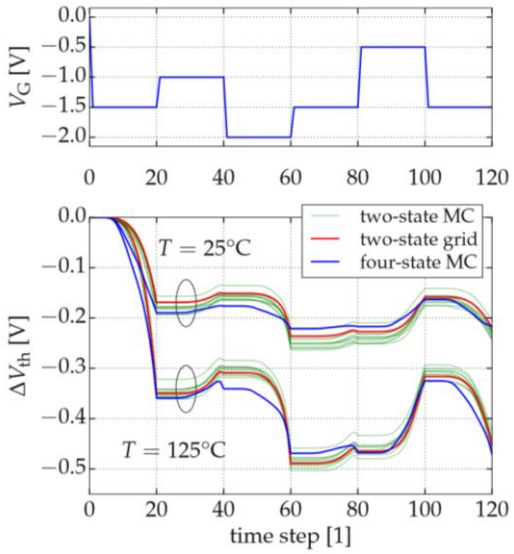


Figure 2.17 - Simulated device degradation (bottom) for a specific gate voltage profile (top). The simple 2-state model captures the overall degradation trend as well as the much more complicated 4-state model. Reprinted from [23].

Since Sentaurus Device internally employs the eNMP model, the simplest way to utilize the 2-state data gathered in WP5 is to “upscale” the simplified model back to a full 4-state model in order to make use of the already existing implementation in Sentaurus Device. This can be done by only using two states (e.g. 1 and 1’) of the implemented eNMP model, with the transition rates to the other states being set to zero. The necessary modification of the Sentaurus Device model can be done by the Physical Model Interface (PMI) in Synopsys Sentaurus Device which allows easy access to the underlying model parameters and rate equations.

3 FDSOI demonstrator – XFirst integration

The second test application described in D6.1 is the FDSOI MOSFET, with XFirst integration, fabricated at CEA-Leti. For the XFirst integration only a planar geometry is considered. Figure 3.1, adapted from D6.1, describes the process flow for the fabrication of the transistors. The XFirst integration FDSOI simulation toolchain has been implemented in Synopsys Sentaurus (Process and Device, release U-2022.12) for pMOS planar devices, as shown in Figure 3.2. For this process flow, *in-situ* doped epitaxial deposition steps are performed after Ge and B implantations as shown in Figure 3.1 (nMOS and pMOS variations are given in green and blue, respectively). The epitaxy step is simulated using the Sentaurus Process LKMC framework, in contrast to XLast integration demonstrators, where `MulSKIPS` was used. Due to the relative low probability of the dopant incorporation events (about 1%), adopting `MulSKIPS`’ resource-intensive KMCsL framework (involving both cubic and hexagonal stacking configurations) does not represent a computationally efficient approach in this case. To have sufficient statistics, larger simulation cells must be used, which would be too computationally demanding in the super-lattice framework. On the contrary, Sentaurus Process’ standard cubic LKMC framework allows for efficient simulations with sufficient statistics for dopant incorporation events. Moreover, Sentaurus Process is equipped with a KMC module for dopant diffusion and

activation which shares the same events table with the epitaxial growth LKMC module, therefore it is well suited to investigate the evolution of impurities during epitaxy.

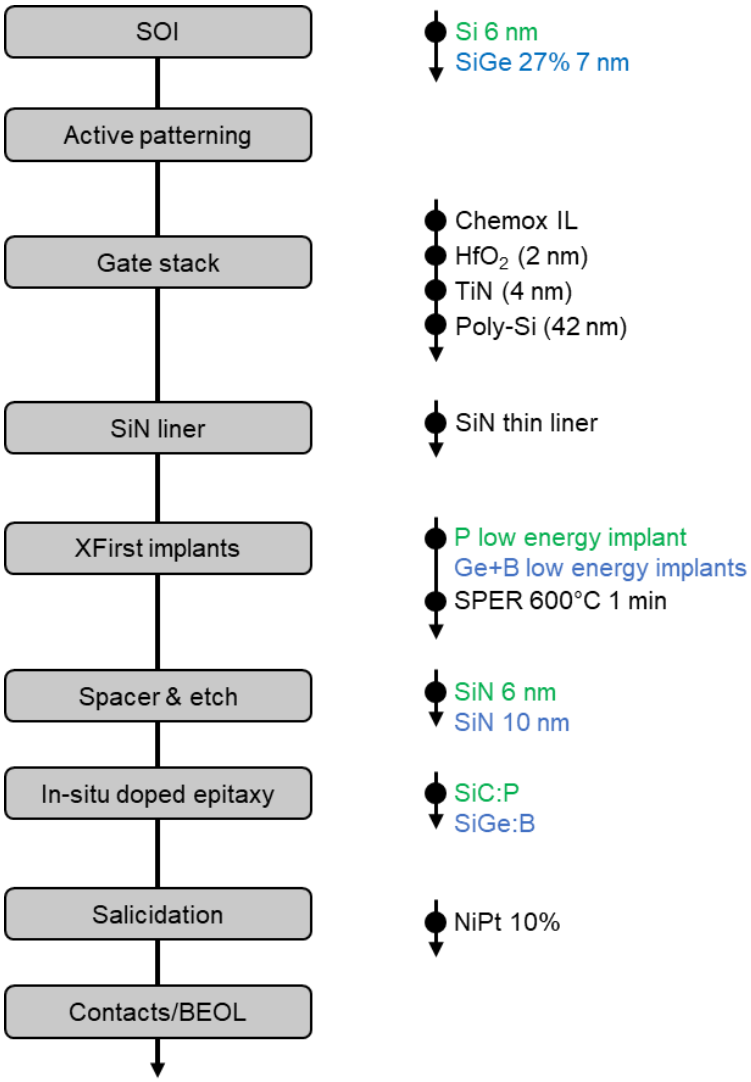
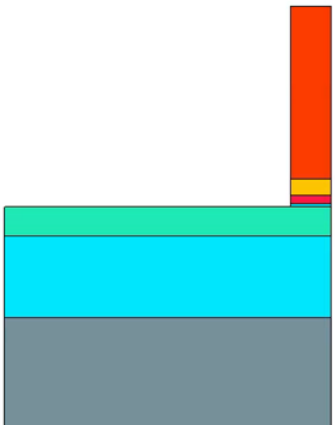
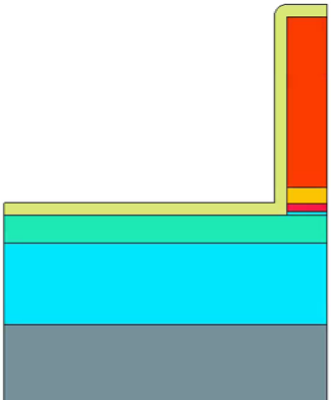
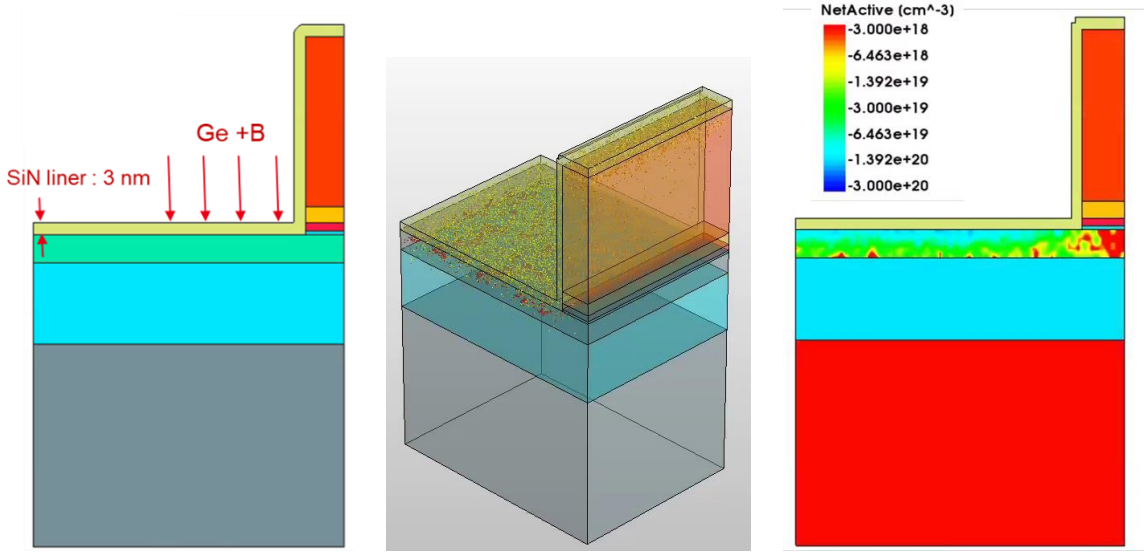
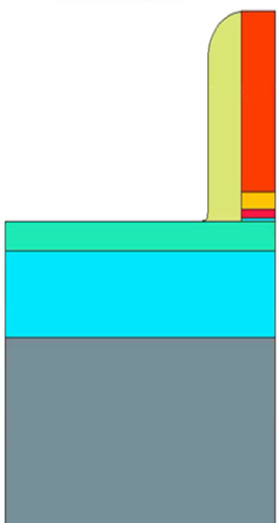
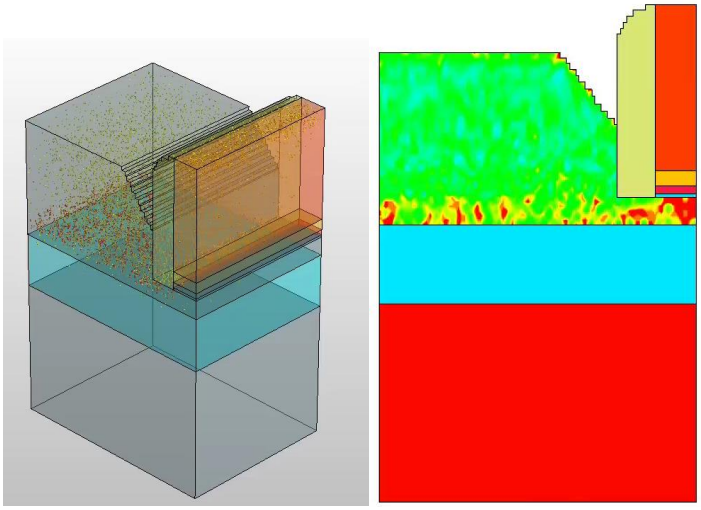


Figure 3.1 - Low thermal budget process flow of an XFirst integration taken from deliverable D6.1 (nMOS and pMOS variations are given in green and blue, respectively).

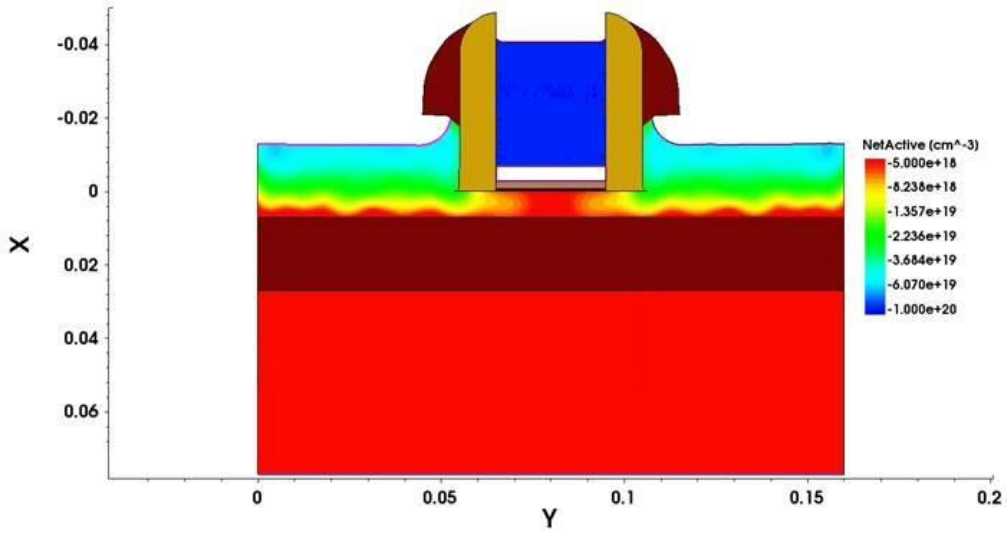
Figure 3.2 - Screenshot of the Sentaurus Workbench project of the full simulation toolchain for the FDSOI device with XFirst integration. The toolchain uses Sentaurus Process and Device (and Visual for visualization).

The different process steps implemented in Sentaurus Process are shown in Table 1 (results are plotted for a gate length of 30 nm).

Table 1 – Process simulation steps for the FDSOI in XFirst integration implemented in Sentaurus Process.

<table>
<tr><td>1. Gate stack patterning
  </td><td>2. SiN liner
  </td></tr>
<tr><td colspan="2">3. Implantations (Ge and B) and SPER (600°C, 60s annealing): KMC simulations
 
</td></tr>
<tr><td>4. Spacer formation
  </td><td>5. In-situ doped SiGe:B epitaxy, LKMC simulations
  </td></tr>
</table>

6. Second spacer formation, silicidation and reflection to obtain full structure and definition of electrical contacts



After remeshing, the final structure obtained after process simulations is used in device simulations, run in Sentaurus Device. The computed transfer characteristics, for linear (dashed line) and saturation regimes (solid line), are shown in Figure 3.3. Simulation of device reliability, applying results obtained in WP5, can be done using the Physical Model Interface (PMI) in Synopsys Sentaurus Device, as described in section 2.3 for the XLast integration.

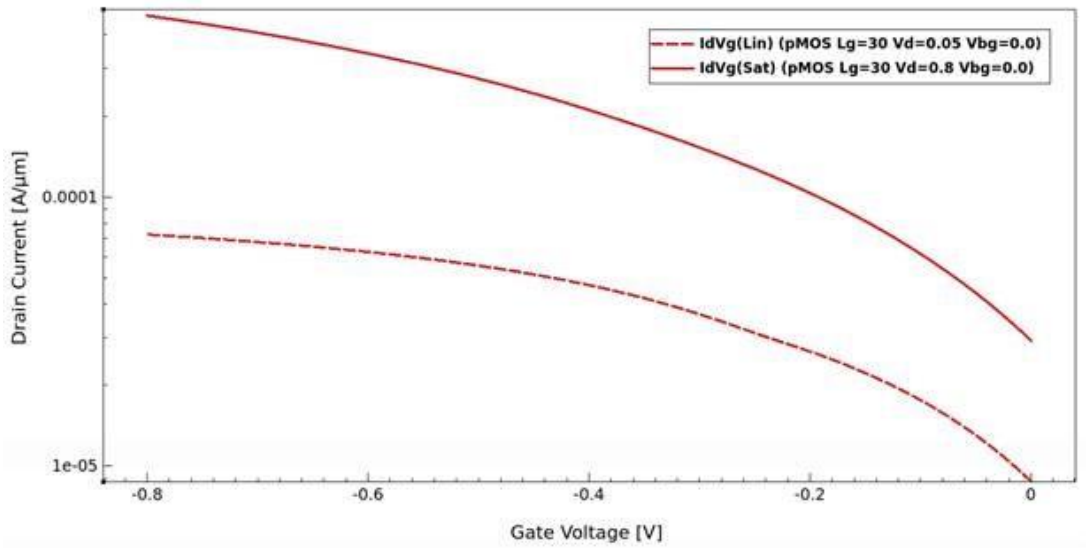


Figure 3.3 - Simulated transfer characteristics for the FDSOI transistor with XFirst integration.

4 Vertical GAA NW-FETs demonstrator

The third test application described in D6.1 is a Vertical Gate-All-Around (GAA) nanowire (NW) field-effect transistor (FET), fabricated by CNRS-LAAS [20, 21]. A TEM image showing a cross section of the fabricated devices is presented in Figure 4.1.a. Figure 4.1.b, adapted from D6.1, reports the corresponding process flow for the complete fabrication of the structure. For this test application, the process simulation of the silicidation step is done in `MulSKIPS`. The extension of `MulSKIPS` capabilities to include atomistic simulations of the silicide formation is the result of the work carried out in WP2, as described in D2.6. Figure 4.1.b schematically summarizes which tools (Synopsys Sentaurus Process [5], Sentaurus Structure Editor [6] and `MulSKIPS` [1]) are used for the different parts of process simulation. The device simulations are then carried out with Sentaurus Device [8], with the inclusion of modelling results from WP5 regarding defects properties in the oxide and at the silicon-oxide interface.

The simulation toolchain starts in the Sentaurus Structure Editor with the definition of the vertical nanowire, patterned by reactive ion etching (RIE), as shown in Figure 4.2.a. The nanowire is obtained from a boron-doped low-resistivity wafer (high constant doping concentration). Then, a first oxidation step is performed in Sentaurus Process. The first oxidation step is a wet oxidation at 850 °C for 5 min and it is needed for nanowire thinning and for removal of residual damage from the etching process. Next, this sacrificial oxide is stripped and a second oxidation is performed to grow the gate oxide (dry oxidation at 725 °C for 20 minutes). The 3D structures resulting from the oxidation steps are shown in Figure 4.2.b (wet oxidation) and Figure 4.2.c (dry oxidation). 2D cuts showing the doping distribution in the nanowire obtained after the oxidation steps are reported in Figure 4.2.e (wet oxidation) and Figure 4.2.f (dry oxidation). It can be noted that the doping distribution in the nanowire is drastically decreased due to boron segregation into the oxide. This effect has to be carefully modeled for a correct prediction of the transistor's electrical behavior. The last step in

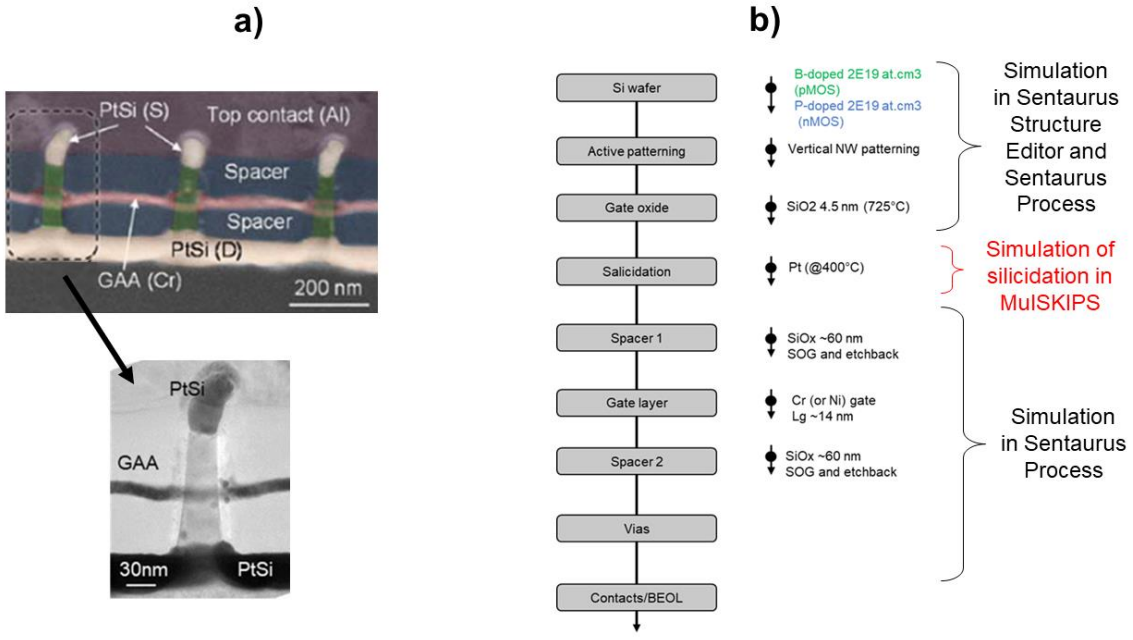


Figure 4.1 – a) Transmission electron micrographs of the vertical nanowire array transistor (cross section in tilted view); b)) Process flow for vertical NW-FET transistors fabrication and corresponding simulation tool used for the modeling.

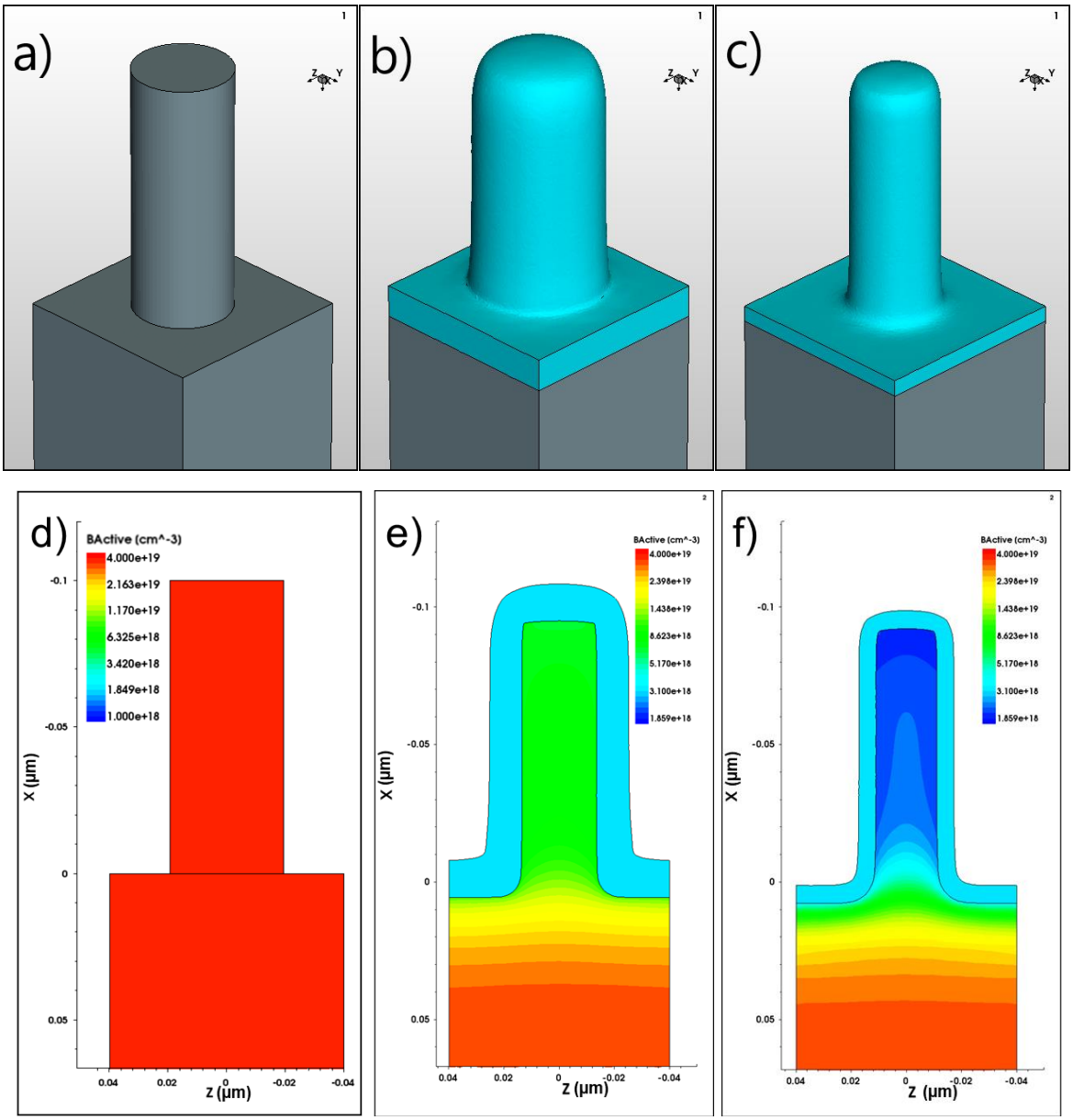


Figure 4.2 – a) Initial nanowire structure (after patterning by RIE) defined in Sentaurus Structure Editor; b) nanowire after simulation of sacrificial wet oxidation in Sentaurus Process; c) nanowire after simulation of dry oxidation (for gate oxide growth); d) 2D cross section of the initial nanowire;); the 2D cross sections of the nanowire after wet oxidation and dry oxidation showing the resulting simulated doping concentration are displayed in e) and f) respectively.

Sentaurus Process is the anisotropic etching of the oxide at the NW top and bottom to expose the silicon surface for the silicide formation.

Full silicidation processes are simulated with an in-cell KMC model integrated, as novel feature, in the `MulSKIPS` framework. Details of the KMC model are reported in D2.6. The model generalizes a Pott-like approach to multi-phase materials and with the participation of elements' diffusing atoms (monomers). Such an approach was previously applied for simulating grains' densification in single phase (single element) metallic nano- and poly-crystalline systems. The key feature of the model is the stoichiometry control of the phase transition as clearly demonstrated by the sequence of Figure 4.3. Here, the simulation starts from a Ni nano-crystalline material, presenting ideal "cubic" grains of Ni with different orientations (indexes from 1 to 10) and a random distribution of diffusing Si atoms with the

correct average density to reproduce the 3:1 (Ni:Si) stoichiometry. Fully periodic boundary conditions are imposed to simulate the bulk material. The system evolves toward the formation of a nanocrystalline stable phase with an averaged stoichiometry of 3:1 stoichiometry, i.e. the Ni_3Si (orientation indexes from 11 to 20). This occurs after an initial reconfiguration of the Ni grains and the formation of a “quasi-amorphous” matrix around the nanograins described in the model by a mixing of different silicides.

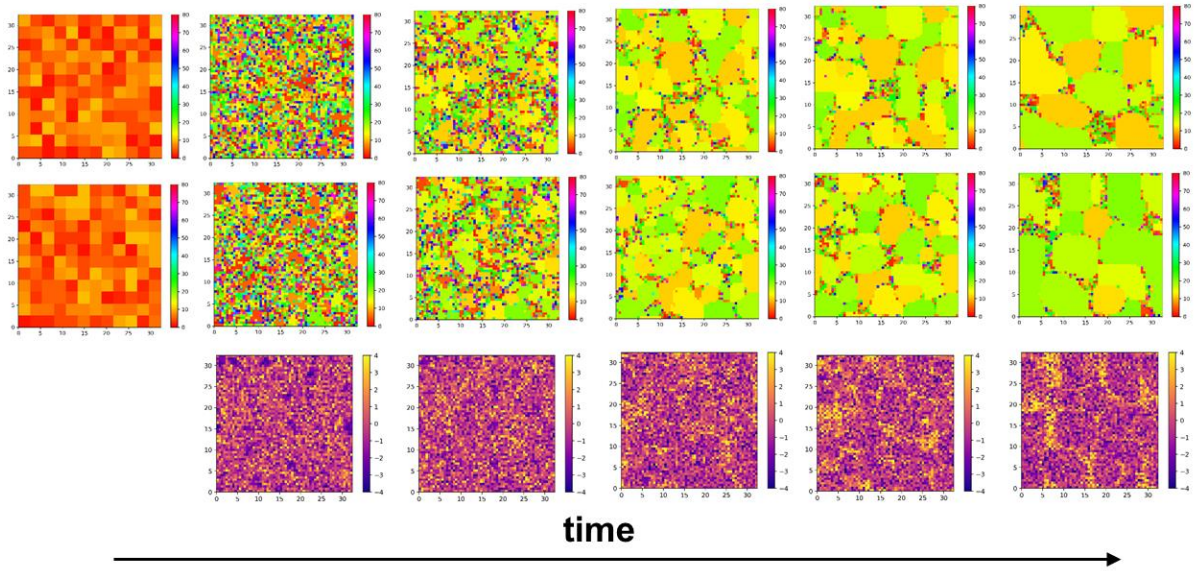


Figure 4.3 - Snapshots of the Ni to Ni_3Si transition. The reaction occurs in a bulk volume prepared as an initial “ideal” nano-crystalline Ni material (cubic and equal sized nanograins) in a “wrong” 3:1 average stoichiometry (i.e. the Ni_3Si one) where all the Si atoms are considered as diffusing ones (the model formulation which also considers Ni and Si diffusing monomers is discussed in D2.6). The system size is a cube of about 33x33x33 nm^3 with periodic boundary conditions. In the top and middle row sequences the grains cross sections along (100) and (010) directions at the simulation box centre are shown. The phase transition from the Ni ideal grains (phase indexes 1-10) and N_3iSi ones (phases indexes 11-20) is indicated by the colour scale. The bottom row represents a deviation of the local correct stoichiometry of the Ni element in a section along (010) direction at the simulation box centre. This parameter is evaluated as the atomic deviation of the Ni element atoms with respect the number of atoms present in the conventional crystal cell of the corresponding phase (see corresponding colour scale in the middle row sequence). ±4 Atoms deviation is allowed in the calibration used here. We notice that this parameter tends to achieve the 0 average value in the bulk of the grains, although fluctuations are possible from cell to cell, while a clear average positive deviation is observed in the grain boundaries’ regions.

This evolution mechanism is common to all the simulated phase transitions. The simulation approach can also be applied to other silicide systems, like the Pt:Si one, and the implemented code can simulate 3D geometry, as needed for the silicon nanowire devices in this demonstrator (see D2.6). 3D simulation results for Ni silicide processing in nanowire geometry, with height and diameter obtained from the oxidations steps in Sentaurus Process (Figure 4.2.c) are reported in Figure 4.4. Here, the early stage of the evolution representing the nucleation of the Ni_2Si phase (orientation indexes from 31 to 40) is analyzed. The test application employs a platinum silicide, as reported in Figure 4.1 and in D6.1. As stated earlier, `MulSKIPS` can also simulate Pt:Si system, so in the final toolchain for model evaluation (D6.4) the platinum silicidation will be considered. The full simulation toolchain presented here can be applied in the exact same way.

After `MulSKIPS` simulations, the results of silicide formation must be imported back to Sentaurus Process, for further processing. The coupling strategy follows what is described in D6.2. `MulSKIPS` provides as output the coordinates of silicon surface nodes obtained from the silicidation step (silicon is in red in Figure 4.4, right side). Unlike the CVD process presented

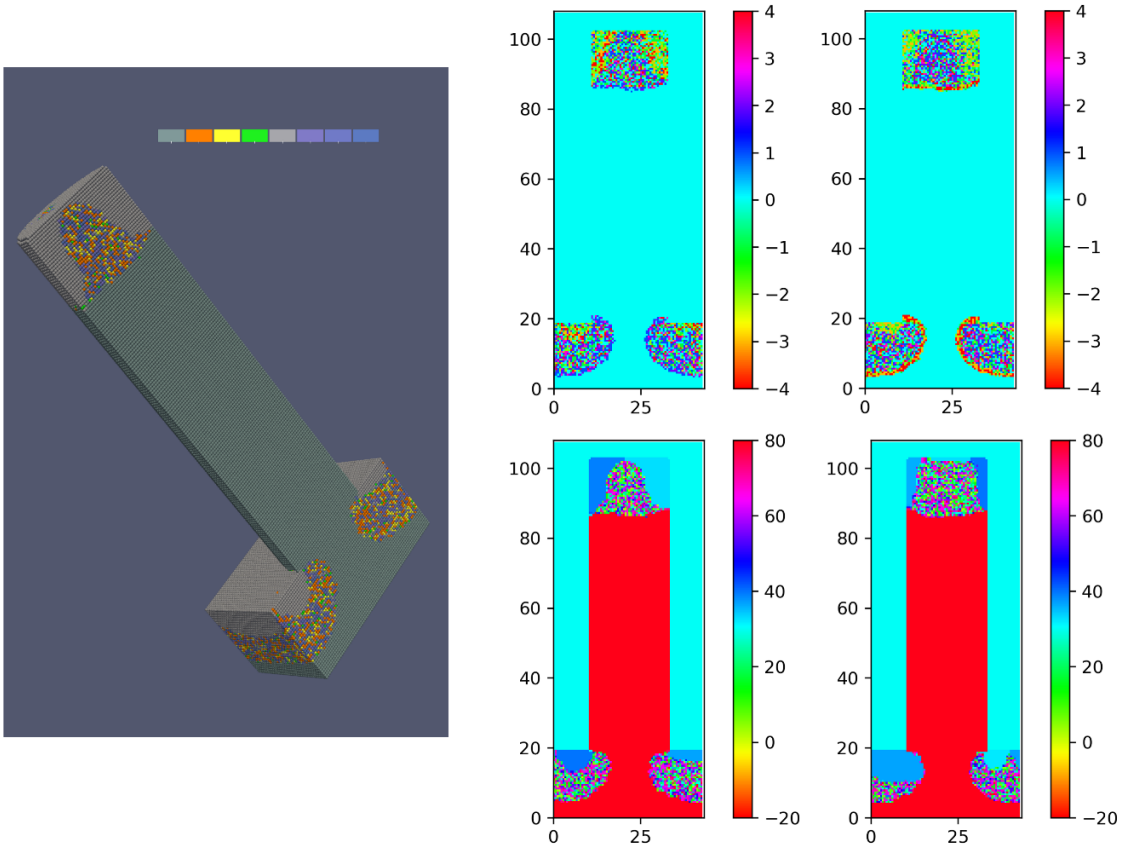


Figure 4.4 - Snapshots of the early stage of silicide process transition in a nanowire structure at the nominal temperature of 260 °C. The simulation box size is a cube of about 40x40x110 nm^3 the light blue region is air. Left hand graph is a snapshot after the nucleation of the Ni_2Si phase (brown regions). The four right hand graphs are: cross-sectional planes of the deviations with respect to the local correct stoichiometry of the Ni and Si elements (Ni top-left, Si top-right, (010) cross sections); and the orientation resolved phases distribution (bottom left (100) cross section, bottom right (010) cross section).

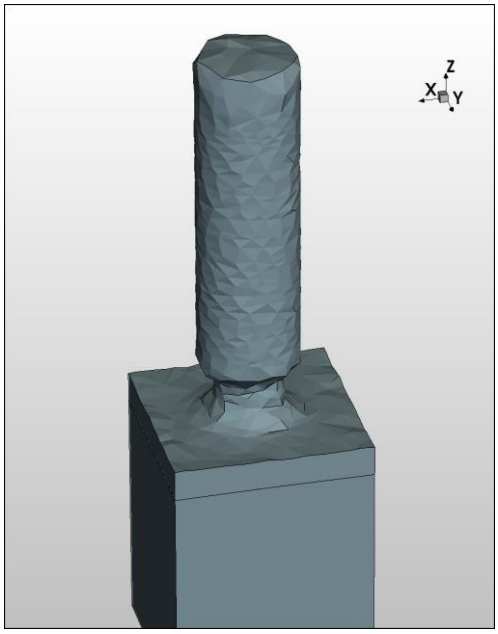


Figure 4.5 – Structure (silicon nanowire) obtained from silicidation simulation in `MulSKIPS` *imported back in Synopsys environment.*

in D6.2, silicidation results in an “etching” of silicon, as part of the material’s transformation into silicide. Since `DEP3D` works as a “deposition” tool, an additional step is needed for a successful application of the coupling procedure, i.e. an extra isotropic etch of the nanowire obtained after oxidation to obtain a surface which is “lower” than the final one after silicidation. Then, `DEP3D` can be used to “deposit” back the surface following the surface nodes from `MulSKIPS` and obtain the correct geometry. The structure of the silicon nanowire obtained from silicidation, and imported back in Synopsys environment, is shown in Figure 4.5 (plotted from a TDR file, i.e. Synopsys internal format). The next steps of the process simulation toolchain are performed in Sentaurus Process starting from the deposition of the silicide material. `MulSKIPS` simulates the formation of different silicides. However, it is common practice for simulations with Sentaurus Device that the silicide

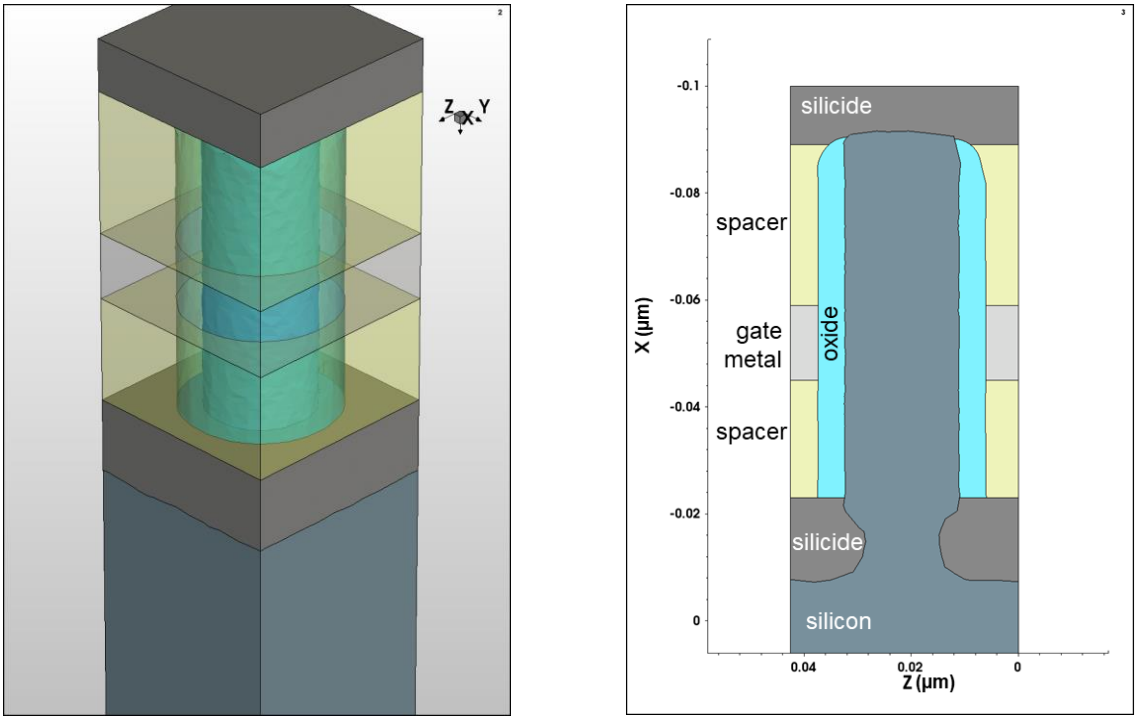


Figure 4.6 – GAA-NW-FET structure obtained at the end of the process simulation toolchain.

region is “substituted” by the electrode region, i.e. the silicide is removed and electrical boundary conditions are applied at the former interface between silicide and silicon. For this reason, the information from the `MulSKIPS` simulation about the different silicides formed is not imported in the geometrical structure, but the effective work function to be applied at the

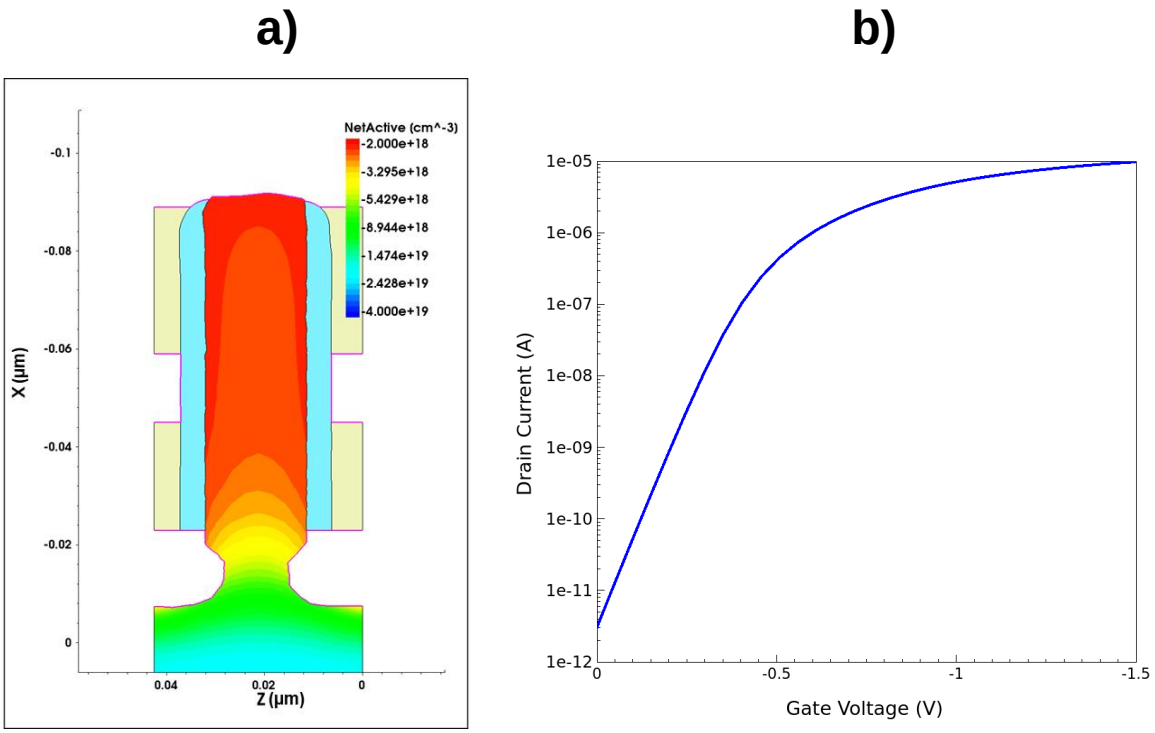


Figure 4.7 – a) Structure used for device simulations. It is obtained from the structure in Figure 4.6. The silicides at source and drain and the gate metal are defined as electrode regions, i.e. the materials are removed and electrical boundary conditions are imposed at the metal/silicon interface (magenta lines); b) transfer characteristics obtained by device simulations for a drain voltage of -0.6 V.

silicide/silicon interface as electrical boundary condition will be defined during device simulations. As a side note, A more detailed information about the silicide may, however, be valuable for next generation device simulators which could take such information into account. Finally, the spacers and gate metal layers are deposited and the final GAA-NW-FET structure is obtained, as shown in Figure 4.6. The 2D cross section, in Figure 4.7.a, features the electrical contacts, highlighted in magenta. This structure is finally used for the device simulations in Synopsys Sentaurus Device, concluding the simulation toolchain. As mentioned earlier, in addition to bias conditions, work functions for the source and drain electrodes, as well as for the gate metal, are specified in the electrode section. The results of simulated transfer characteristics, for a drain voltage of -0.6 V (boron-doped nanowire), gate metal work function of 4.2 eV and drain/source Schottky contact work function of 5.2 eV, are shown in Figure 4.7.b. We note that results of atomistic simulations from WP5, to study device reliability, can be included also in this toolchain, as for the FDSOI demonstrators. The approach employing the Physical Model Interface (PMI) in Synopsys Sentaurus Device, described in section 2.3, applies also here. The complete advanced simulation toolchain, including external atomistic tools, presented in this deliverable, will be evaluated against experimental results and benchmarked with respect to the standard simulation approaches in D6.4.

5 Demonstrator for Laser Annealing

Although laser annealing (LA) is not present in the process flow for the fabrication for the test applications presented in D6.1, advanced simulations of LA are a core activity of the MUNDFAB project, with the whole WP4 dedicated to that. The combined theoretical and computational advancements that were reached during the MUNDFAB project represent the state-of-the-art of laser annealing simulation in group IV semiconductors and alloys. In particular, a novel hybrid atomistic-continuum methodology has been developed, as described in D4.8, which allows the combined use of atomic resolution for particle kinetics and continuum representation of thermal and electromagnetic fields generated during the laser anneal process [22, 3]. This methodology has been implemented in the external tool `MulSKIPS` [1].

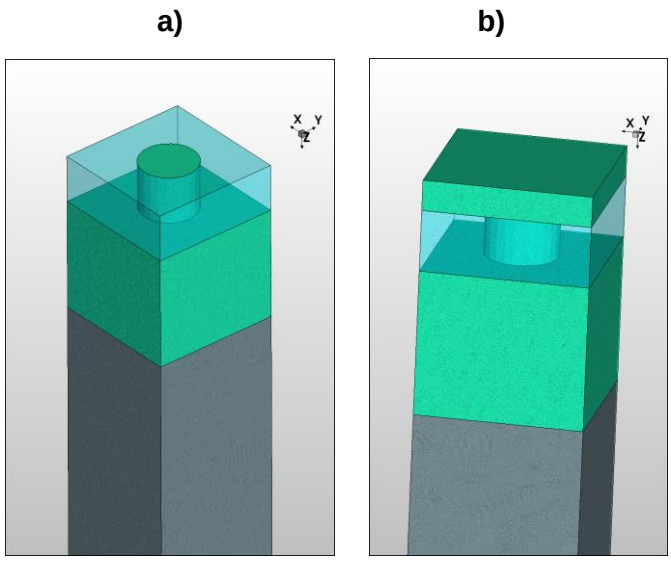


Figure 5.1 – Initial structures, obtained in Sentaurus Process, that will be used in `MulSKIPS` for laser annealing simulations: a) without capping layer on the $Si_{0.6}Ge_{0.4}$ nanowire and b) with capping layer on the $Si_{0.6}Ge_{0.4}$ nanowire.

In order to demonstrate and fully exploit the capabilities of the developed simulation approach, it is beneficial to integrate them in a simulation toolchain for a complete process flow. For this reason, we present here an additional fourth demonstrator to show the integration of LA `MulSKIPS` simulations within the Synopsys Sentaurus environment. The demonstrator consists of a 9-nm-large and 10-nm-high $Si_{0.6}Ge_{0.4}$ nanowire (NW) on top of a 30-nm-thick strained $Si_{0.6}Ge_{0.4}$ thin film on a ~20-µm-thick Si substrate. The NW is embedded into SiO_2, which does not melt during the irradiation and represents a

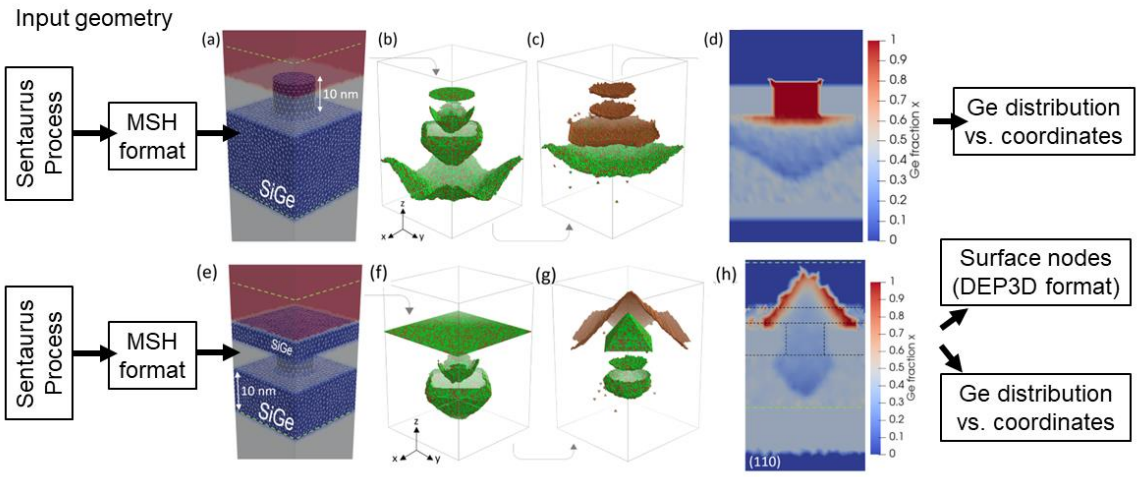


Figure 5.2 – Scheme for coupling of advanced hybrid LA and Synopsys Sentaurus. (a-e) Results of LA simulations refers to an irradiation (308 nm, 22 ns, 0.95 J cm^{-2}) of a 30nm-thick strained $Si_{0.6}Ge_{0.4}$ on a ~20 µm-thick Si substrate, with nanowires on top, embedded into hard non-melting SiO2 mask. (e-h) LA simulations (308 nm, 22 ns, 1.2 J cm^{-2}) for the same structure above, but with an additional 5nm capping layer of $Si_{0.6}Ge_{0.4}$; a/e) initial FEM mesh, periodic along x and y, with KMCsL-coupled SiGe regions in blue, air in red, oxide and non-KMCsL-coupled regions in grey; b/f) overlapped selected snapshots showing the liquid-solid interface in the KMCsL box at various instants during melting; c/g) interface during solidification, including the final surface morphology; d/h) (110) cut plane of the structure- after LA, with colours indicating local Ge content.

geometrical constraint for the evolving solid-liquid interface. A variation of this structure, including a thin (5 nm) capping layer of $Si_{0.6}Ge_{0.4}$ on top of the NW and oxide regions, is also considered, to study atomic scale reshaping in the solidification stage. The initial structures are generated using Sentaurus Process [5] and are reported in Figure 5.1. A 200-nm-thick layer of air (not shown in Figure 5.1) is also included in the mesh. The coupling procedure to obtain a MSH file from a TDR file, exploiting an intermediate step through GRD file, as described in D6.2, is then applied. The MSH file is used as input in `MulSKIPS` for the LA simulation (hybrid atomistic-continuum methodology, as mentioned above and described in D4.8). In particular, a laser pulse with 308 nm wavelength, ~22 ns duration and energy density of 0.95 J cm^{-2} (1.2 J cm^{-2} for the NW with capping layer) is considered. Figure 5.2.a/e reports the initial FEM mesh for the two structures. Blue regions indicate SiGe regions which will be mapped into KMCsL. Red regions indicate air and grey ones indicate SiO_2 and the remaining SiGe/Si region lying beneath the KMCsL mapped region. The KMCsL box is 27 x 27 x 41 nm and includes the top ~23 nm of SiGe, the NW, the oxide and ~8 nm of air. In Figure 5.2.b/f few snapshots at different time steps of the melting liquid-solid interface are plotted. To stabilize the initial stage of melting, an initial 1.5 nm thick layer of liquid SiGe is assumed at the beginning of the LA simulation. For the structure without capping layer (Figure 5.2.b), the initial interface is circular in this case, because the first (and only) part of the surface exposed to the laser is the tip of the NW. As the NW absorbs heat, it melts all the way down to the substrate. After the complete melting of the NW, the molten phase assumes a tetrahedral shape in the region below the oxide. The kinetics of the subsequent solidification is reported in Figure 5.2.c. The almost planar interface evolves towards the initial surface level while constrained by the oxide. Ge segregates and solidifies later, causing a total transformation of the initial SiGe nanowire into a pure Ge nanowire. This Ge distribution in the structure at the end of the LA simulation is plotted in Figure 5.2.d ([110] cut-plane). A slight tendency of solidifying the edge NW areas before those in the centre can be noticed in the final KMCsL snapshots, which is

emphasized in the FEM Ge map due to the larger mesh resolution (more details on these simulations can be found in D4.8). The KMCsL evolution of the solid liquid interface of the structure with capping layer is illustrated in Figure 5.2.f-g. The laser energy density used in this case is sufficiently low to avoid coalescence of molten nuclei below the oxide region. As a result, solidification begins with a non-planar shape. As soon as the solid seed emerges above the oxide, it rapidly assumes a highly symmetric pyramidal shape, with facets along the [111] directions. The pyramid enlarges while concurrently segregating Ge, until it partially coalesces with its periodic replicas and a uniform thin Ge layer covers the final solidified surface, as shown in the map of the Ge distribution in Figure 5.2.h (more details in D4.8). The final simulated structures must then be transferred back to the Synopsys Sentaurus environment. For the case of a NW without capping layer (Figure 5.2.d), the final topography was not modified during LA, as there are just some negligible differences, so the part of the coupling procedure involving `DEP3D` can be skipped. The important step in the coupling procedure for this test application is the import of the new Ge distribution resulting from the LA simulations. `MulSKIPS` gives as additional output a text file which contains the local Ge concentration as a function of coordinates in the entire mesh. As described in D6.2, Synopsys TDR mesh files can be converted to DF-ISE format, i.e. ASCII files (so editable): one in GRD format for the mesh and one in DAT format that stores the physical data fields. Based on the `MulSKIPS` output text file containing Ge concentration, the physical data fields are imported into the DAT file. This is done using a Python script developed within the project, which updates the physical data values in the DAT file by carrying out a nearest-neighbour mapping of the data stored in the `MulSKIPS` output text file. The GRD and the new DAT file are then converted to TDR format, which can be further processed in Sentaurus Process or Device, using the Sentaurus Data Explorer. The final structure, visualized in the Synopsys Sentaurus environment with Sentaurus Visual, is reported in Figure 5.3. The structure with capping layer on top of the NW undergoes a significant topography change after LA, as it can be seen in Figure 5.2.h. In this case, the full coupling procedure, including `DEP3D` first and then the import of physical data fields, must be followed. The final structure after the coupling procedure, visualized in Synopsys Sentaurus Visual, is reported in Figure 5.4.

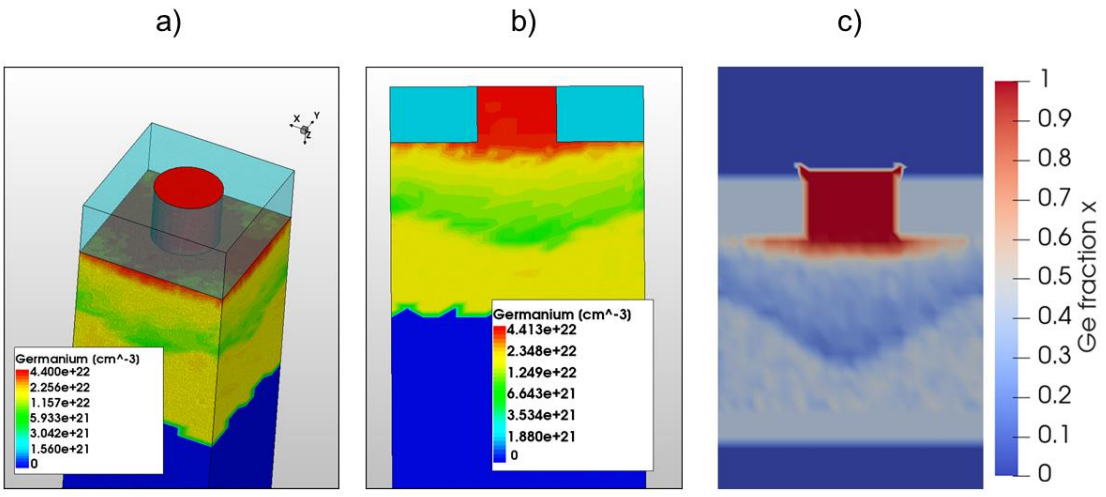


Figure 5.3 – a) Final structure, resulting from `MulSKIPS` LA simulations for the structure without capping layer (as in Figure 5.2.d), after the coupling back to TDR format in Synopsys Sentaurus environment; b) 2D cut of the structure for comparison with Ge fraction (c) from Figure 5.2.d.

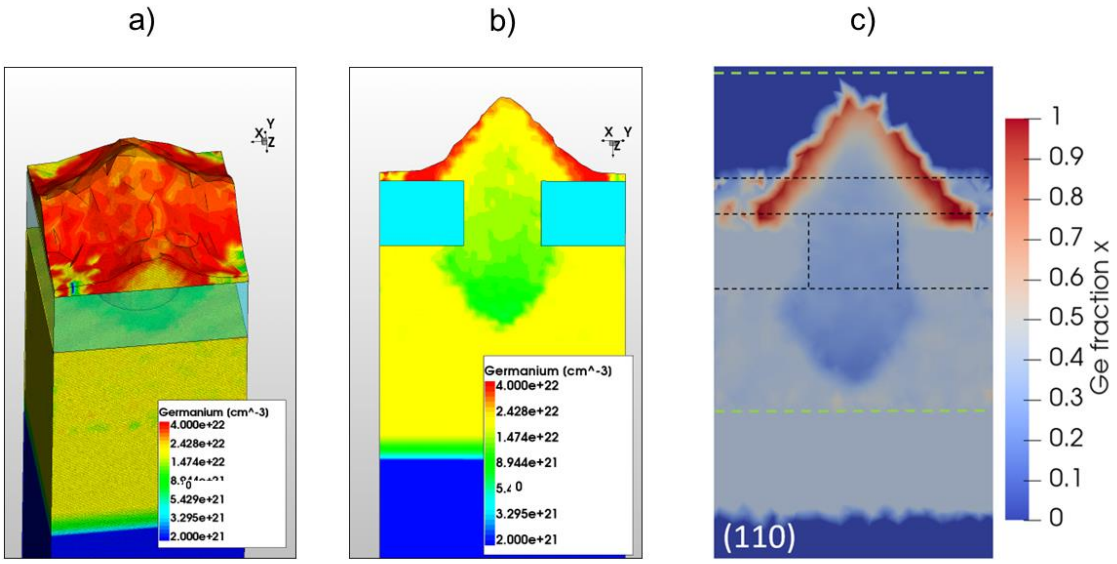


Figure 5.4 – a) Final structure, resulting from `MulSKIPS` *LA simulations for the structure with capping layer (as in Figure 5.2.h), after the coupling back to TDR format in Synopsys Sentaurus environment; b) 2D cut of the structure for comparison with Ge fraction (c) from Figure 5.2.h.*

These results confirm the possibility of a full coupling of `MulSKIPS` LA simulations and Synopsys Sentaurus TCAD.

6 Conclusions

This deliverable describes the full simulation toolchains developed for the process and device simulations of the test applications, including novel results developed in the other work packages (WPs from 2 to 5) of the project. The simulation toolchains mainly run within Synopsys Sentaurus but use also the external in-house simulations tools, in particular the external KMCsL tool `MulSKIPS`, which include the novel modelling advancements developed in the project. `MulSKIPS` (modelling results of WPs 2 to 4) has been integrated in the toolchains following the coupling strategy presented in D6.2. The final device simulations also integrate the results of WP5, in which an off-lattice kinetic Monte Carlo method and DFT calculations are used. Simulation toolchains for the test applications described in D6.1 were presented, i.e. FDSOI devices fabricated in XLast and XFirst integration and a GAA-NW-FET. Moreover, an additional test application was reported to demonstrate the possibility of the integration of WP4 results in a more general simulation toolchain. The toolchains presented here will be evaluated against standard modeling approaches and experimental data in D6.4.

7 References

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