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MUNDFAB

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**MUNDFAB**
Modeling Unconventional Nanoscaled Device FABrication

# D2.5: Final experimental results on silicidation of Si and SiGe bulk materials and nanowires

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## Quality management

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## Contents

## Abstract

In this deliverable the shared experimental results from CNR-IMM and LAAS-CNRS obtained within **Task 2.3** of **WP2** are presented. Firstly, available information from the literature on the silicidation and phase transformation for the Ni/Si and Pt/Si binary alloys as well as ternary (Pt)Ni/Si and Ni/SiGe systems is reviewed. The early stages of the silicidation process have been studied and compared for the Ni/Si and Pt/Si systems by CNR using in-situ X-ray analyses (XRD, XRR) on blanket samples, characterizing different stages of the process and the atomic structure of layers with different crystalline phases. Further, the effect of different thermal annealing processes on observable phases has been highlighted by comparing blanket samples obtained after rapid thermal annealing at LAAS. The electrical measurement of the bulk Ni/Si silicide sheet resistance has been demonstrated as a reliable and fast technique to characterize silicide thin films. Based on previous experiments of PtSi on Si-nanowires at LAAS, the silicidation of NiSi on nanowires has been studied in detail by structural and chemical characterization trough transmission electron microscopy and energy dispersive X-ray analysis (HR-TEM, STEM/EDX). As a means to further improve the observed interface formation of nanostructured Ni-Si, the silicidation of NiPt on nanowires has been implemented. A first demonstration of the Ni silicidation on plain and nanostructured SiGe is also provided.


## 1 Introduction

Metallic silicides are metal-silicon alloys that are formed through solid-state reactions or diffusion processes of the two materials (silicide process). These metal-semiconductor alloys combine the stability of silicon and the low resistivity of metallic materials. Conventional processes are based on a metal deposition on silicon, followed by thermal annealing which activates the reaction of the two materials. Different silicides, such as $CoSi_2$ or $TiSi_2$ provide good electrical properties and were thus a key component for the fabrication of nano-metric contacts of electrical devices such as MOSFETs. These first silicides have however been replaced over time by other silicides such as NiSi and PtSi which outperform their predecessors' electrical properties and allow for silicidation at lower temperatures with a lesser silicon consumption during the reaction.

PtSi, finds application as ohmic or Schottky barrier contacts for MOS and CMOS but is also heavily relied upon as contact material for e.g. infrared detectors and other micro-electronic systems thanks to its high thermal stability. The Pt-Si system is well studied and understood in parts thanks to a simple silicidation reaction with few Pt-Si phases.
NiSi provides good electrical properties (a low resistivity of down to 10.5 μΩ·cm), mechanical stability, low Si consumption, and decreased tendency to agglomerate as compared to other silicide contacts.
Thus, NiSi is a highly interesting silicide for the continuous down-scaling efforts of the semiconducting nanoelectronics industry and particularly for future CMOS applications. However, the Ni-Si system exhibits more phases in its silicidation sequence as compared to Pt-Si and, despite many recent research activities, is not fully understood yet (see for example [1]). One important aspect is the improvement of the stability of the desired low resistive NiSi phase and thus to avoid the formation of highly resistive Ni-rich or Si-rich phases. The industrial self-aligned silicidation process (salicidation) requires a thermal annealing process in the range of 400-700 °C depending on the annealing method such as conventional furnace annealing (CFA) or rapid thermal annealing (RTA) and the contact (metal film thickness, nanostructuring, etc.).

## 1.1 Goal of this deliverable

One of the main goals of **Task 2.3** is the fabrication of nanostructured low-resistive NiSi contacts on highly vertical nanowire structures while optimizing the salicidation with respect to a decreased thermal budget. Vertical nanowires are seeing more and more application in the fields of vertical nanostructured Field Effect Transistor (FET) or nanowire-based dynamic random-access memory (DRAM) devices as they offer ultimate scalability if fabricated through a top-down approach [2-4]. Furthermore, relying on a vertical nanowire platform also provides a simple-to-implement possibility of stacked device fabrication along the nanowires. Reliable and symmetric silicide contacts are a crucial technological component for the realization of future CMOS devices or more complex 3D structures, managing multiple devices, or creating logic cells by stacking. Especially for stacked devices, the thermal budget has to be reduced because high-temperature salicidation effectively causes thermal aging of underlying contacts by every subsequent anneal. Prolonged thermal annealing will cause unwanted phase transformations and eventually electrical failure of the contacts and devices. It is thus important to understand the impact of thermal annealing as well as the geometric constraints on the phase transformation of nanostructured contacts.

We thus present the progress on the investigation of the Ni-, Pt- and NiPt-silicidation conducted at CNR-IMM and LAAS-CNRS as part of the MUNDFAB project. **Section 1.2** entails a brief summary of relevant information concerning the Pt-Si, Ni-Si, and NiPt-Si systems used in the initial investigation of bulk silicides in **Chapter 2**. **Section 2.2** highlights the investigation of the early stages of silicidation as characterized by in-situ X-ray diffraction and reflectometry at CNR-IMM while **Section 2.3** presents electrical characterization results of rapid thermal annealing samples. A detailed investigation of Ni-Si silicidation of vertical silicon nanowires as characterized by transmission electron microscopy and energy dispersive X-ray analysis is given in **Chapter 3**. Finally, **Chapter 4** provides a first demonstration of the characterization of germane-silicide contacts, presenting the first results on the nickel silicidation on SiGe nanowires based on the fabrication techniques presented in the deliverable **D4.6**.

## 1.2 Review of silicidation with Ni, Pt and NiPt in the literature

This section provides a short review of the available literature on the silicidation process of nickel and platinum silicide contacts as well as their alloys.

*Platinum silicidation*

The Pt-Si salicidation is a simple reaction that is dominated by two major transitions corresponding to the phase transition from Pt-Si to $Pt_2Si$ at 270-300 °C and successively from $Pt_2Si$ to PtSi at 320-340 °C depending on film thickness and annealing conditions [5, 6]. Though it is not commonly observed during self-aligned silicidation, some sources (e.g.[6, 7]) report on the observation of $Pt_3Si$ forming as an early stage, thus at low temperatures down to room temperature, during growth or successive processing. Alternatively, $Pt_3Si$ can be directly grown through e-beam co-evaporation [8].

The Pt-Si phase diagram of [9] is presented in **Appendix 1.1 Figure 20a** and displays the 5 stable and metastable phases (listed in **Appendix 1.1 Table 3**) and the RTA silicide evolution as observed by Larrieu et al. [6] shown in **Appendix 1.1 Figure 20b**.

PtSi provides a low resistivity and excellent thermal stability of up to 700 °C. For higher temperatures, PtSi starts to degrade by dissolving increasing amounts of silicon [10] leading to agglomerations. This has also been associated with the formation of voids in the PtSi by

Das et al. [11]. In both cases, the observed instabilities are caused by an activation of Pt diffusion from the PtSi layer into the underlying silicon substrate.

### *Nickel silicidation*

The Ni-Si phase transformations are well known for high-temperature processes, as shown by the phase diagram of [12] in **Appendix 1.2 Figure 21**, and displays 11 stable and metastable phases of which 7 are stable at room temperature [13] (see **Appendix 1.2 Table 4**). From an industrial point of view, the goal is to form the low resistive mono-silicide NiSi while avoiding the silicidation of nickel-rich phases such as $Ni_2Si$ (200-350 °C, [14]), the highly resistive silicon-rich $NiSi_2$ phase appearing for high-temperature processes of around 550 °C or higher [13-15]. NiSi thus appears as the dominant phase for processing temperatures between 350-550 °C [15] but can be observed, depending on the annealing duration, for higher temperatures as well [13, 14, 16]. Common silicidation processes of Ni have thus been carried out at an annealing temperature of around 500 °C for a few minutes to obtain a fully transformed NiSi contact.

During the silicidation reaction, Ni is the initial diffusing component that enters the substrate. Thereby firstly forming Ni-rich phases such as $Ni_2Si$, commonly observed for conventional furnace annealing as presented in **Figure 1b** even though Ni-rich phases such as $Ni_3Si$ are expected to be formed first during RTA [17], and finally NiSi. However, the conventional Ni-silicidation sequence is largely simplified as intermediate phases such as the high resistive $Ni_{31}Si_{12}$ and $Ni_3Si_2$ may appear depending on the thermal processing conditions during silicidation. Further, if for example $Ni_{31}Si_{12}$ is formed, it may not directly transform into $Ni_2Si$ but simultaneously forms $Ni_2Si$ and $Ni_3Si_2$ reducing the mismatch stress in the system [18]. Further annealing may then result in only a partial rather than a complete NiSi silicidation see e.g. [19]. It is thus necessary to verify the phase transformation sequence from the literature, which is mostly obtained with traditional annealing techniques, for other annealing conditions and techniques.

### *Ni silicidation with Pt additive or NiPt alloys*

While the above-stated temperature ranges are correct for thick nickel layers, the obtainable Ni-Si phases in thin films depend also on the deposition conditions of the nickel film as well as the presence of dopants in the system. The Ni diffusion is impacted by the grain size of the Ni film as well as the amount of dopants that hinder it within the substrate [20]. For decreasing film thickness the Ni grain size limits the formation of NiSi due to the internal stresses developing in the film or causes a partial transformation [21]. Smallest thin films eventually completely suppressed NiSi transformation [22].

While the impact of e.g. boron dopants in the substrate has no significant influence on the silicide formation and its properties (arsenic causes a slight slow-down of the transformation) [23], the silicidation can be severely impacted by the presence of alloys in the metal.

The addition of selected materials to alloy the metal-silicide can thus be used to tailor the contact transformation during silicidation. An ideal alloying element for the optimization of nickel-based contacts is Pt which was first introduced because it delays the formation of $NiSi_2$ and limits the NiSi agglomeration [24]. A relative improvement of 10 nm thick NiPt to pure Ni contacts obtained by rapid thermal annealing on arsenic doped silicon was presented in [25], extending the thermal stability of the mono-silicide phase from 650 to 800 °C.

Due to the low solubility of Pt atoms in $Ni_2Si$, they segregate into the NiSi lattice replacing Si positions with a tendency to move towards the interfaces. The addition of 10% Pt thus leads to a thicker NiSi layer as well as a sharper $Ni_xSi_y$ profile at the contact substrate interface due

to the stabilization of the nickel monosilicide phase [26], while also acting as diffusion barriers [27].

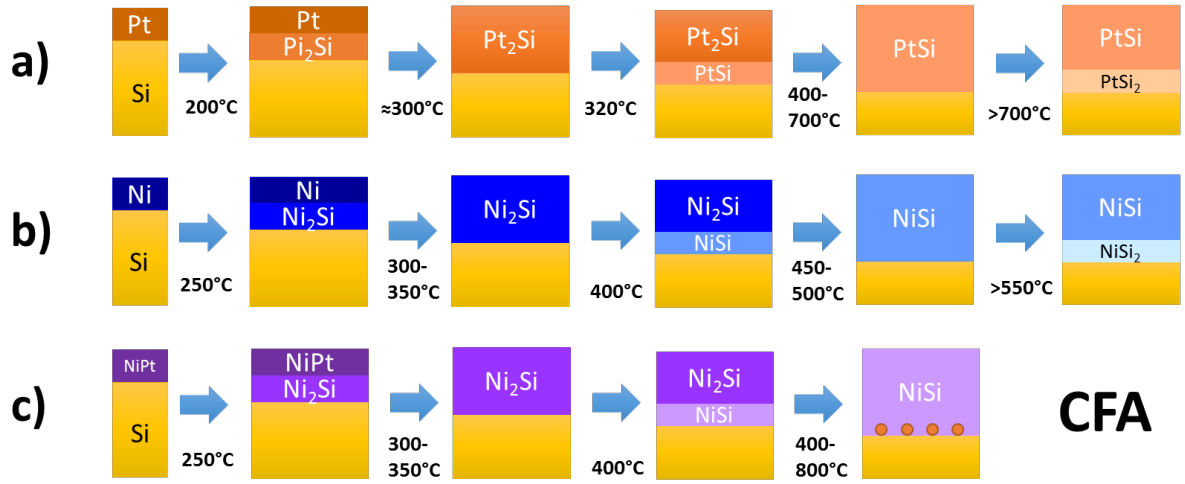



**Figure 1: Schematic representation of the phase evolutions during silicidation of (b) Ni-, (a) Pt- and (c) NiPt-silicide systems as prepared by conventional furnace annealing (CFA).**

## 2 Bulk silicidation of Ni, Pt and NiPt on Si substrates

Here we present the investigation of bulk silicides such as Ni, Pt and NiPt fabricated by PVD and different annealing techniques such as conventional furnace annealing (CFA) applied for the in-situ X-ray measurements of the early silicidation stages of both Ni-Si and Pt-Si, conducted by the CNR-IMM as presented in **Section 2.2**, and the rapid thermal annealing (RTA) that is commonly used for the contact annealing in industrial process as well as the nanowire contact fabrication at CNRS-LAAS. RTA sample results and their electrical characterization are presented in **Section 2.3**.

### 2.1 Metal deposition and thermal processing

The starting wafers are 4” (100) p-Si bulk wafers, lightly doped (Boron at $1 \cdot 10^{15}$ at/cm). The wafers were first cleaned in Piranha ($H_2SO_4$:$H_2O_2$ 1:1) solution to remove any organic residues on the surface. Secondly, the native silicon oxide layer of 1-2 nm thickness was removed by wet chemical etching in diluted Hydrofluoric acid (HF(5%):Methanol 1:1) for 30 s. The acid is diluted in methanol in order to follow the same process that is used for the preparation of silicon-nanowire (NW) samples which are also planned to be fabricated for WP2. Silicon-NWs have to be rinsed/etched in methanol rather than in water as its high surface tension may break the wires during the drying-process. Then, the wafer was immediately placed under vacuum in an electron-beam evaporator “Plassys MEB-550SL” to minimize the re-formation of the native oxide layer. An optional in-situ Ar milling was performed prior to the metal deposition. The Ar plasma was obtained at a 5 sccm flow of Ar with a chamber pressure of $6.5 \cdot 10^{-5}$ mbar for 2 min. Some test samples were fabricated without the in-situ Ar-milling step. The deposition of 10 nm of nickel or platinum occurred at a low deposition rate of 0.1 nm/s, at room temperature without any additional heating and with a beam power loading of 280 mA and 10 kV.

Alternatively, for the deposition of NiPt alloys with 10% Pt, the wafer was placed under vacuum in a PVD magnetron sputtering system “AC450CT”. An in-situ Ar milling step prior to the metal deposition was conducted with an Ar plasma at 200 W for 1 min. The deposition of 10 nm of

NiPt at a moderate deposition rate of 0.8 nm/s, at room temperature without any additional heating was achieved for a power of 300 W during 12 s.

The metalized wafers were retrieved from the evaporator or sputtering system and stored within an $N_2$ locker before being cleaved and either being further processed by rapid thermal annealing RTA at LAAS-CNRS or being transferred to the “Institute for Microelectronics and Microsystems (IMM)” in nitrogen filled and hermetically sealed containers for the in-situ thermal annealing and X-ray characterization (XRD, XRR).

### *Conventional furnace annealing (CFA)*

The in-situ X-ray diffraction (XRD) and X-ray reflectometry (XRR) measurements were conducted by placing the as-deposited sample in a dome heating stage under dry nitrogen conditions for reference measurements and in-situ annealing. After an initial measurement at 30 °C, the samples were annealed using an annealing and measurement protocol as shown in **Figure 2a**. The protocol includes three consecutive annealing steps at 260, 300, and 380 °C with a heating rate of 1 °C/sec in between segments. Each temperature was held for 1 h before cooling down the samples to 30 °C in order to record XRD and XRR in between each segment. The entire measurement procedure results in a total annealing time of ca. 3.5 h per sample (including the initial heating and final cooling step). All diffraction patterns were recorded using a Goebel mirror at the primary beam and a scintillator at the secondary beam (Bruker D8 Discover).

### *Rapid-thermal annealing (RTA)*

The rapid thermal annealing process used for electronic devices and nanostructures produced at LAAS-CNRS relies on the AS-One rapid thermal annealing system from AnnealSys. Samples were placed within a SiC-coated graphite susceptor in the process chamber which was firstly evacuated and then filled with forming gas (3% $H_2/N_2$) for the thermal process. After gas activation and thermalization, an initial ramp up to 10 °C below the set point with a rate of 15°C/s was followed by a second ramp up to the process temperature in order to minimize any PID overshoot of the temperature during the annealing step. After the main process had finished, the sample was left to cool down under a nitrogen atmosphere for a few minutes.

Silicide samples were prepared at temperatures ranging from 200-800 °C for annealing times of 0.5-10 minutes. Lower annealing temperatures are not achievable as the PID overshoot, as for example for 100 °C and 2 min as shown in **Figure 2b**, cannot be reliably controlled.

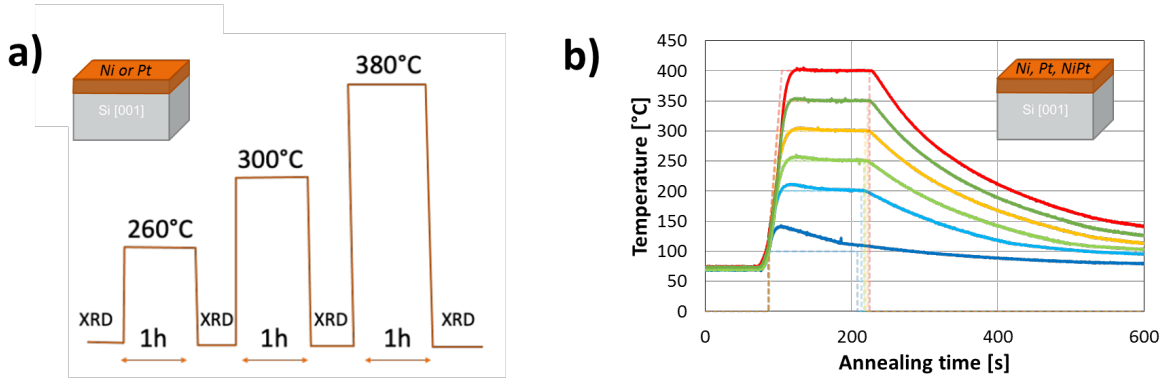



**Figure 2: Heating curves for the different annealing techniques used for the silicidation of bulk samples. (a) In-situ annealing for the XRR/XRD characterization under nitrogen atmosphere. The samples are successively heated up to different temperatures for an hour and measured at 30 °C in between ramps. (b) Rapid thermal annealing in a lamp oven under forming gas $N_2/H_2$ atmosphere. Shown are temperature curves for processes at 100-400 °C.**

## 2.2 Experimental results on the early stages of Ni and Pt silicidation

Nickel thin film samples have been fabricated as described in **Section 2.1** for the in-situ silicidation putting a special focus on the detailed characterization of the as deposited material and its interface with silicon by X-Ray Reflectivity (XRR) analyses combined with High-Resolution Scanning Transmission Electron Microscopy analyses (HR-STEM). XRR is an analytical technique sensitive to the electronic density of the materials and indeed well suited to finely describe eventual Ni-Si intermixing and phase formation.

### 2.2.1 Early stages of Ni-Si interaction

**Figure 3 (left)** shows the XRR profile of the as deposited sample with typical interference fringes that are related to the layer thickness. The critical angle measured on that profile corresponds to a density of 8.9 g/cm$^3$. A nickel layer is indeed found in the topmost part of the sample with thickness close to 8 nm. This value underestimates the deposited thickness. Accordingly, a description of a pure nickel layer on top of a silicon substrate is not exhaustive to properly fit the experimental curve. A refined model of the sample includes a second layer in touch with the silicon substrate, as described in the inset of the figure. It consists of a 3 nm-thick Ni-Si mixed layer with a density of 8 g/cm$^3$, which corresponds to a Ni:Si ratio of 3:1.

A similar scenario was depicted by HR-STEM analyses as shown in the cross-section of the as-deposited sample of **Figure 3 (right)**. The topmost layer of nickel is made of nanometer-sized grains that are mostly [111] oriented. A mixed layer is found immediately under the pure nickel layer as introduced by XRR. As additional information, this layer has a low degree of lattice order (similar to an amorphous one).

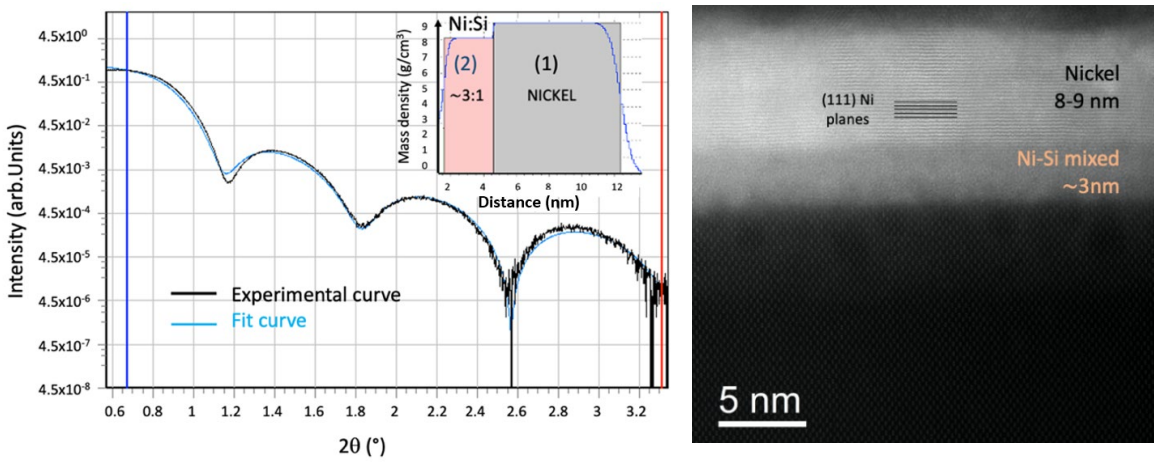



**Figure 3: XRR profile of the as deposited Ni/Si sample (left), with the schematic of the layered structure and composition in the inset and HR-STEM cross-section of the as deposited Ni/Si sample (right).**

Ni-Si mixing with similar features was previously found in samples wherein the nickel layer was deposited by sputtering [28]. Since by evaporation the adatoms are less energetic than the ones produced by sputtering, it is argued that intermixing occurs independently of the adatoms' energy through a mechanism of adsorption-diffusion-injection mechanisms as described in the theoretical dissertation reported in this report. In addition, the observed Ni-Si mixing in a ratio of 3:1 found by XRR and HR-STEM corroborates a driving force for nickel insertion into the silicon lattice with a description provided by the theoretical calculations.

### 2.2.2 Ni/Si silicidation process in the range 260-380 °C

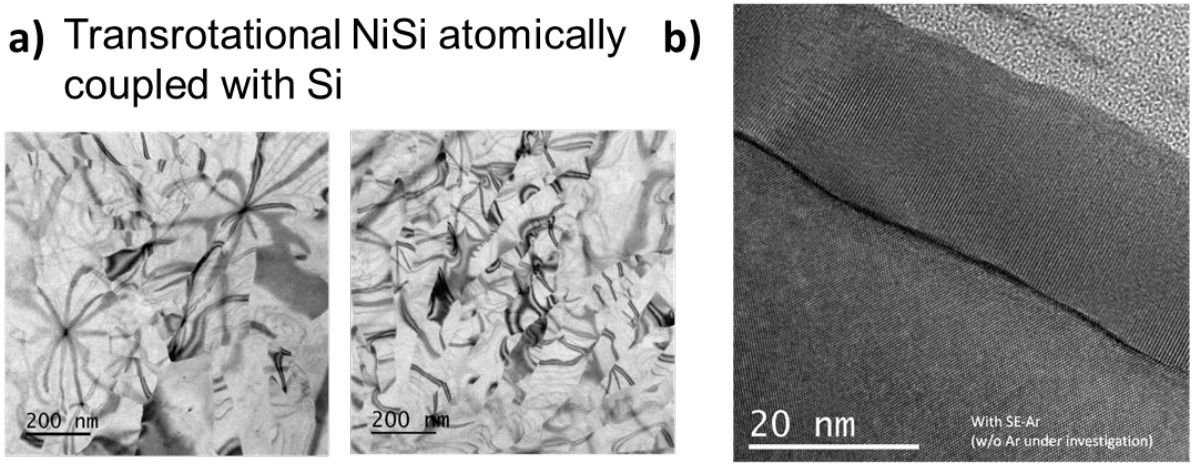



**Figure 4: Plan-view and cross-section of the Ni-silicide film reacted by the annealing protocol illustrated in Figure 2a.**

Mixing of Ni and Si species since the early stages of the deposition process is a phenomenon that pre-sets a pathway for further reaction. A large overview of how this occurs can be found in the review paper "A. Alberti and A. La Magna, Journal of Applied Physics **114** (12), 2013" [28]. With respect to that reference paper, the experiment under MUNDFAB adds insights into the use of evaporation for setting an initial mixing between Ni and Si species similar to what was previously found by sputtering.
It has been in addition disentangled that mixing occurs similarly with and without applying a step of ion sputtering to the pristine silicon surface (in both cases a chemical etching to remove the native oxide is applied). Mixing Ni-Si atoms at the early stages enables a possible reaction pathway that results in a strong coupling between the silicide layer with its orthorhombic lattice and the silicon substrate with its cubic lattice, thus establishing a special kind of atomistic match at the interface. This coupling generates silicide grains with transrotational lattice arrangements (see [28] for full description). Transrotational silicides were formed in the MUNDFAB samples by applying a stepwise protocol as that one depicted in **Figure 2a**. The fingerprint of the transrotational NiSi formation is the habit of the silicide grains with their crossing fringes (bending contours). Transrotational grains are highly oriented (textured), structurally uniformly (high inner lattice order) and with interfacial Schottky barriers lower than in random polycrystalline layers with the same stoichiometry. Transrotational NiSi grains are shown in the high-resolution image of **Figure 4 (right panel)**.

### 2.2.3 Pt/Si silicidation process in the range 260-380 °C

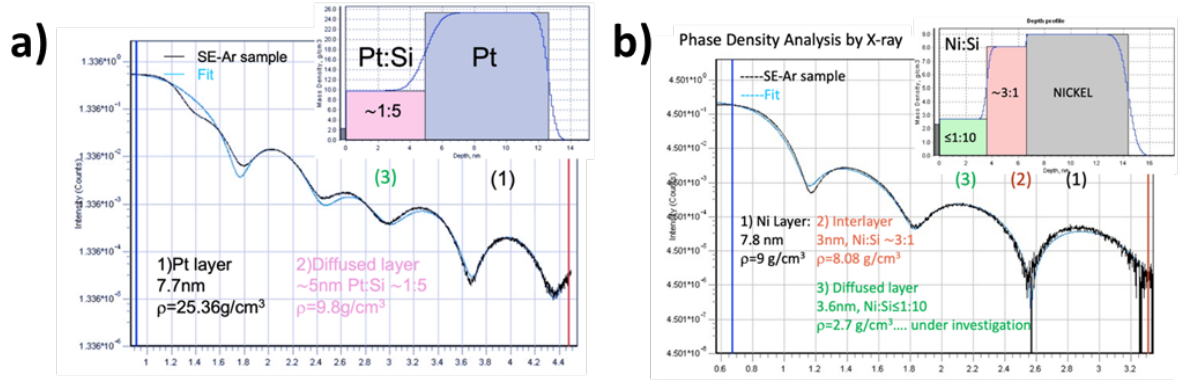



**Figure 5: XRR profiles of the two Pt (left) and Ni layers (right) deposited on silicon.**

Pt deposition was performed on silicon by evaporation and the silicidation was induced by applying the same protocol as the one used for nickel. Hereafter a comparative study is reported.

**Figure 5** and **Table 1** show the two X-ray Reflectivity profiles and the related fitting parameters that evidence the difference between the two materials. A certain degree of mixing is found also in the Pt/Si sample but with less amount of Pt atoms involved.

**Table 1: XRR summary of Pt/Si samples**

**Summary**

PLATINUM

| | As deposited | 260°C-1h+300°C-1h+380°C-1h |
|---|---|---|
| Layer thickness and density | 8 nm<br>25g/cm³ | 22 nm<br>13g/cm³ |
| Diffused layer<br>Pt:Si~1:5 | ~ 5 nm<br>10g/cm³ | ~4 nm<br>5-6g/cm³ |

NICKEL

| | As deposited | 260°C-1h+300°C-1h+380°C-1h |
|---|---|---|
| Layer thickness and density | 8 nm<br>9g/cm³ | 20 nm<br>5-6g/cm³ |
| Mixed layer | 3nm<br>8.1 g/cm3 | / |
| Diffused layer<br>Ni:Si~1:3 | ~4 nm<br>2-3g/cm³ | 2-3 nm<br>2-3g/cm³ |

The protocol for reaction to trigger silicidation used for Pt/Si is used likewise for Ni/Si. The results of the diffractometric analysis are shown in **Figure 6** and summarised in **Table 2**.

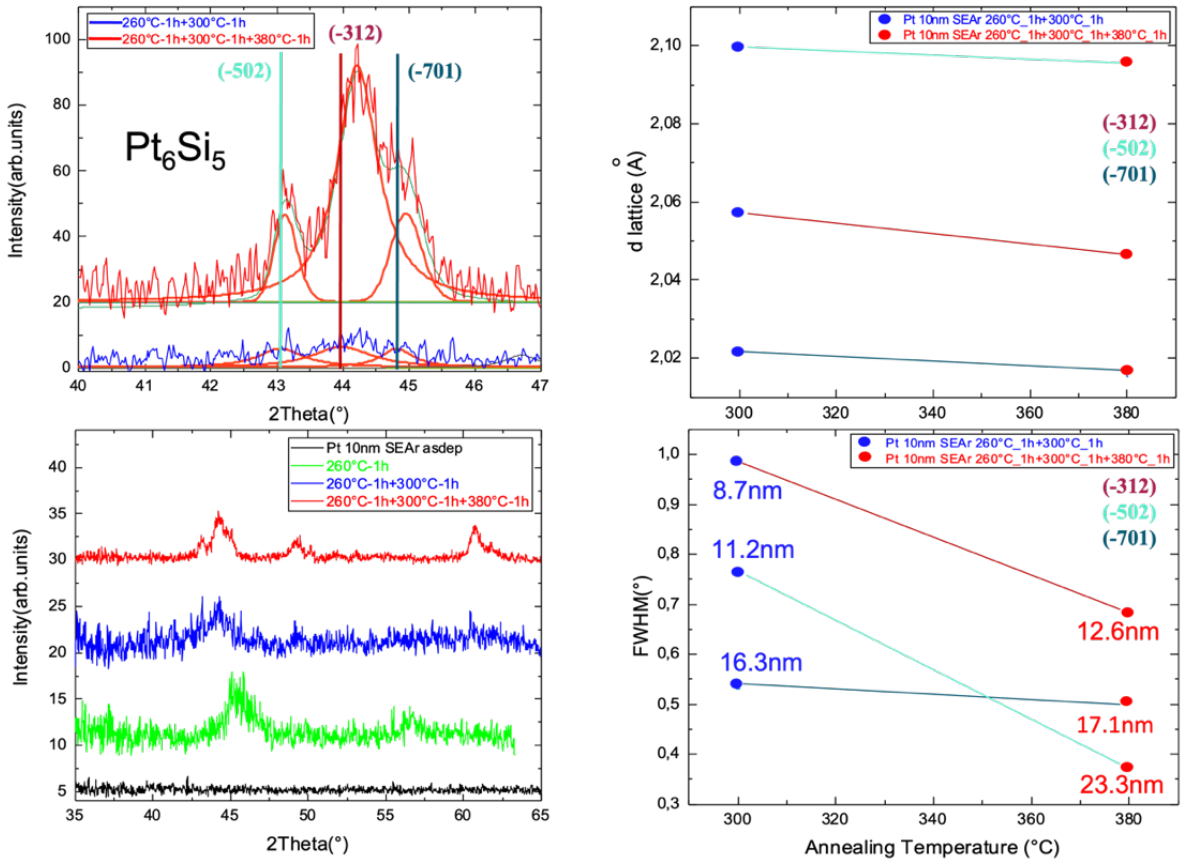



**Figure 6: XRD data on Pt/Si samples reacted following the protocol in Figure 2a.**

The diffraction patterns in the left panels of **Figure 6** provide evidence of the progressive formation of a $Pt_6Si_5$ phase by increasing the temperature (protocol in **Figure 2a**). The right panels show a slight contraction of the lattice spacing (d) at the main crystallographic planes of the $Pt_6Si_5$ phase and a corresponding shrinkage of the peaks full width at half maximum (FWHM) while increasing the reaction temperature from 300 °C to 380 °C (all diffraction patterns are taken at room temperature after annealing). All those findings imply a ripening/coalescence of small grains with partial release of the accumulated strain.

**Table 2: XRD summary of Pt/Si samples**

**Summary**

PLATINUM

| | 260°C-1h+300°C-1h | 260°C-1h+300°C-1h+380°C-1h |
|---|---|---|
| d-spacing | Ref. | < |
| Grain (cry) size | Ref. | > |

From 380°C: $Pt_6Si_5$ as main phase

NICKEL

| | 260°C-1h+300°C-1h | 260°C-1h+300°C-1h+380°C-1h |
|---|---|---|
| d-spacing | Ref. | < |
| Grain (cry) size | Ref. | > |

From 260°C to 380°C: NiSi as main phase

A comparison of the project results to a typical reaction path as illustrated in **Figure 1a** is reported in the literature by G.Larrieu et al. [6] shown in **Appendix 1b**. In addition to the reported case, the formation of a $Pt_6Si_5$ phase before PtSi stabilization at temperatures above 400 °C is documented. Its presence has the drawback of increasing the resistivity of the film to a high value (170 µΩ cm) with respect to PtSi (30-40 µΩ cm) as reported in [29]. Its presence may explain the eventual unexpected rise in resistive contributions.

The application of the same reaction protocol for Ni and Pt reactions on silicon finally allows concluding that Pt-silicidation is a slower process than Ni-silicidation for a fixed reference stoichiometry (e.g. metal:silicon=1:1). Mixing is reasonably a driving force to promote silicidation, with its particular setting at the early stage being able to tune the structural properties of the reacted layer.

## 2.3 Electrical characterization of bulk silicides created by RTA

In this section, we presented the electrical characterization of bulk silicides fabricated by the same rapid thermal annealing process that is utilized for the silicide contact fabrication on nanostructured devices (see for example [4]). The electrical characterization of bulk samples serves as both a reference measurement for the electrical properties of the nanostructured contacts, which are not easily measurable without additional fabrication steps and a means to characterize the phase transformation in the bulk silicide by comparing the measurement results to known resistivities of the silicide phases from the literature (see **Appendix 1.1 and 1.2**). This allows to compare the impact of the rapid thermal processing on the silicidation process as compared to traditional annealing furnaces (CFA). All presented sheet resistance values were measured at room-temperature with a CMT-SR2000NW 4-probe station and the results were manually corrected with the geometry factor of the individual samples.

### 2.3.1 Sheet resistance measurement of bulk silicides

*Results for platinum-silicide*

Multiple samples of Pt silicide have been prepared on 2·2 $cm^2$ chips with an initial Pt layer of 11.8 nm, deposited by PVD as described in **Section 2.1**, with an as-deposited resistivity of 31.3 µΩ cm. The samples have been annealed under different conditions and the sheet resistances were measured by the 4-probe technique with the results presented in **Figure 7**.

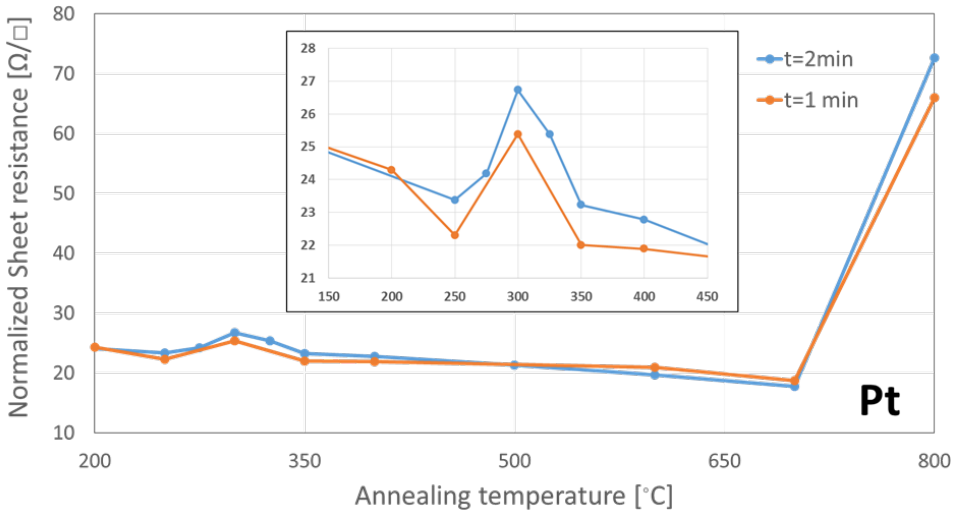



**Figure 7: Normalized sheet resistance of bulk platinum-silicides measured by the 4-probe technique. Initial deposition of 11.8 nm Pt on 2·2 $cm^2$ substrates has been transformed into silicide by rapid thermal annealing at different temperatures in the range of 200-800 °C for 1 and 2 min.**

The results show a low resistivity plateau from 350-700 °C corresponding to the mono-silicide phase PtSi. Considering the theoretical PtSi thickness of 23.6 nm based on the known silicide/metal thickness ratio (see **Appendix 1.1 Table 3**), one obtains a low resistivity of 52.2 μΩ cm which agrees well with the literature [30]. For higher temperature, the sheet resistance increases drastically as the silicide-rich phase is formed. For lower temperatures of 200-350 °C, a peak in the sheet resistance is observed which corresponds to the formation and transformation of $Pt_2Si$ to PtSi.
Surprisingly, increased anneal times lead to an overall increase in the sheet resistance for annealing temperatures below 500 °C while it is decreased for longer anneal times at temperatures of 500-700 °C. This is different than what is observed for nickel-silicide.

### *Results for nickel-silicide*

Likewise, samples of nickel silicide have been prepared on 2·2 $cm^2$ chips with an initial Ni deposition thickness of 10.4 ± 0.3 nm. The as-deposited resistivity of the nickel layer is measured as 22.1 μΩ cm. The samples have been annealed at different temperatures and durations before being measured with a 4-probe station. The obtained normalized sheet resistances are presented in **Figure 8**.

After an initial spike in the sheet resistance due to the formation of high-resistive Ni-rich phases such as $Ni_{31}Si_{12}$, the results show a large plateau for the low resistive NiSi phase (8.3 Ω/□) from 350 to nearly 600 °C. For higher temperatures, the highly resistive Si-rich $NiSi_2$ phase is formed. As observed by SEM images of the silicide surface, the formation of $NiSi_2$ causes the formation of agglomerated grains/zones. This formation is already visible at the onset of the transformation around 600 °C, while the Ni-Si structure is dominated by fine grains for lower temperatures. As presented here for annealing times of 1 and 2 minutes, the initial NiSi transformation peak is shifted to a lower temperature for higher anneal times. It has been verified that NiSi can be formed for temperatures as low as 300 °C for annealing times of 10 min.

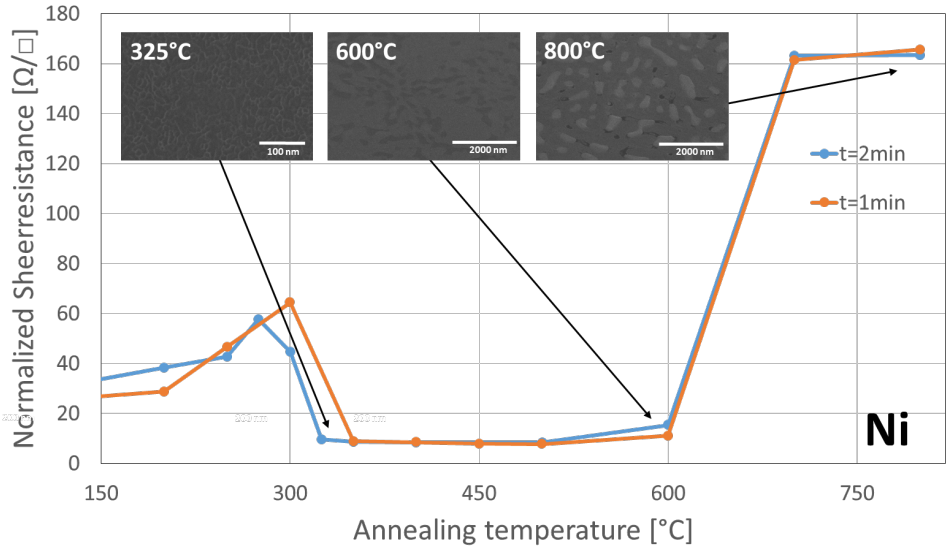



**Figure 8: Normalized sheet resistance of bulk nickel-silicides measured by 4-probe technique. 10.4 nm thick Ni layers on 2·2 $cm^2$ substrates have been transformed into silicide by rapid thermal annealing at different temperatures in the range of 200-800 °C for 1 and 2 min. Selected SEM images of the surface morphology of Ni-Si at 325, 600, and 800 °C are shown as insets.**

*Addition of 10% Pt to nickel-silicidation*

Another option to extend the NiSi plateau is the addition of Pt or using Ni-Pt alloy contacts. To verify the stabilizing properties of the mono-silicide Ni-Si phase as presented in **Section 1.2**, a 24 nm thick NiPt (10% Pt) alloy layer was created on 2·2 cm$^2$ chips by sputtering deposition. The measured thin film resistivity of NiPt as-deposited is 61.1 µΩ cm. These samples have been annealed at different temperatures for the set duration of 1 minute as a preliminary test. The measured sheet resistances are presented in **Figure 9**.

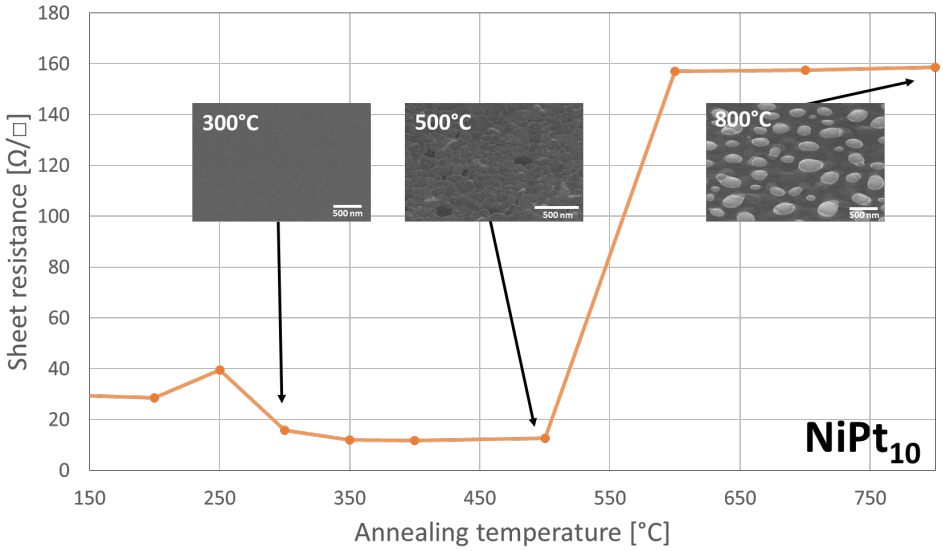



**Figure 9: Sheet resistance of bulk nickel-platinum-silicides measured by 4-probe technique. 24 nm thick NiPt with 10% platinum on 2·2 cm$^2$ substrates has been transformed into silicide by rapid thermal annealing at different temperatures in the range of 200-800 °C for 1 min. Selected SEM images of the surface morphology of NiPt-Si at 300, 500, and 800 °C are shown as insets.**

Based on the results, we determine that the mono-silicide NiSi plateau is observed from 300 to around 550 °C. While the transition from NiSi to $NiSi_2$ is not directly observed it is expected to be between 520-580 °C. In consequence, for NiPt layers of this thickness, we cannot observe any delay of the $NiSi_2$ formation as compared to pure nickel–silicide contacts of 10 nm thickness.

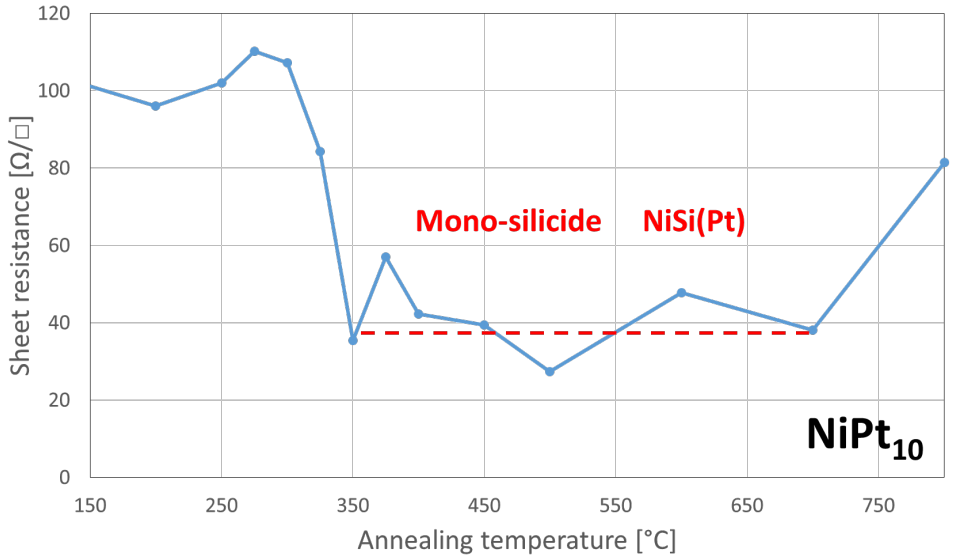



**Figure 10: Sheet resistance of bulk nickel-platinum-silicides measured by 4-probe technique. 10 nm thick NiPt with 10% platinum on 2·2 cm$^2$ substrates has been transformed into silicide by rapid thermal annealing at different temperatures in the range of 200-800 °C for 2 min.**

As thin-film thickness may have an increased impact on the formation of $NiSi_2$, the test is repeated for an adjusted film thickness of 10 nm. The samples have been annealed at temperatures of 200-800 °C for the set duration of 2 minutes and the measured sheet resistances are presented in **Figure 10**. As indicated in red, the mono-silicide (NiSi) plateau is stabilized, as expected, from 350-700 °C for thin layers of NiPt alloys.

### 2.3.2 Silicide characterization through electrical measurement

While the identification of phases such as low-resistive mono-silicide phases is obvious, the knowledge of the resistivity of individual metal-silicide phases allows a more detailed prediction of a sample's composition. This is especially interesting for Ni-Si systems where more intermediate phases than in the Pt-Si system may appear. Under the assumption that the complete thin film has transformed into silicide and that only two phases exist at the same time, the measured sheet resistances taken from **Figure 8** can be modeled as follows:

$$\frac{1}{\rho_1/t_1} + \frac{1}{\rho_2/t_2} = \frac{1}{R_{\blacksquare}}, \qquad (1)$$

Where $\rho$ represents the known resistivity of the phases as listed in the Appendix (see **Appendix 1.2 Table 4** for Ni-Si) and $t_{1/2}$ are the respective thicknesses as calculated from the initial metal film thickness and the known silicidation ratios $t_{film} \cdot r_{sil}$.

Based on the literature, the dominant phases of the Ni-Si contacts have been determined as shown on the annealing curves in **Figure 11a**. To validate this approach, selected samples have been observed by TEM and compared to the predictions. The cross-sections of two samples of Ni-Si bulk samples annealed at 300 and 400 °C for 1 min are shown in **Figure 11b**. Both samples display two separate phases, as well as an oxide layer near the surface, whose composition has been analyzed by EDX line-scans.

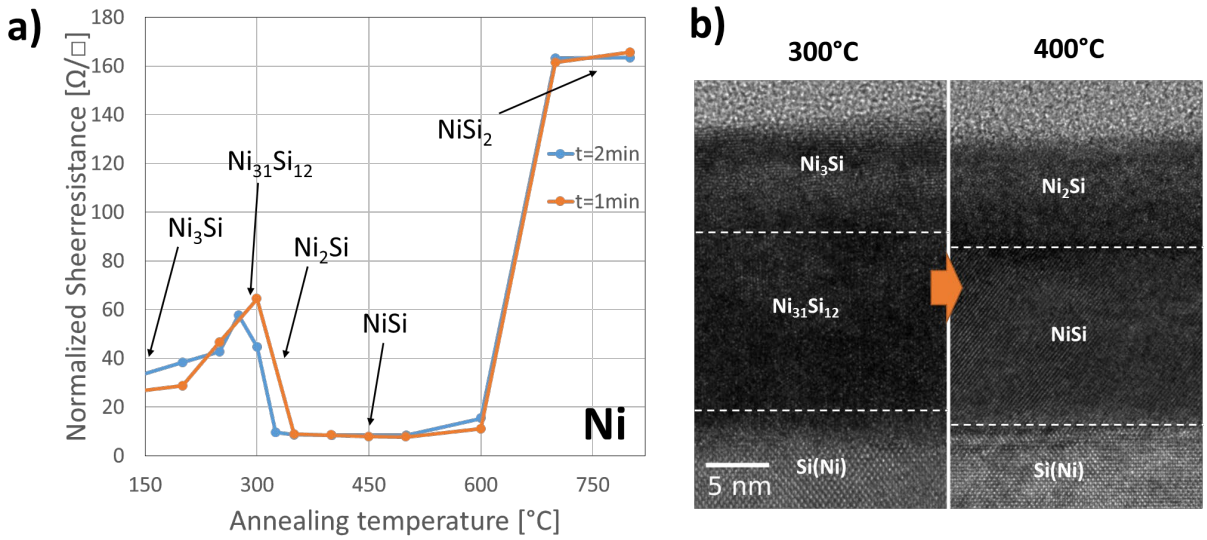



**Figure 11: Characterization of the Ni-Si phase transformation sequence based on the measured sheet resistance (a) and a complimentary TEM observation and EDX analysis of selected samples (b). The estimated dominant phases as determined by the measured sheet resistances have been noted in (a) while the phases in (b) have been determined based on obtained stoichiometries from EDX measurements. With both methods in good agreement, the estimative characterization method of bulk silicide samples based on their electrical properties has been validated.**

In the case of 300 °C, for the first layer, a majority phase of $Ni_{31}S_{12}$ is expected and confirmed by EDX. The smaller top layer, however, also being superposed by the surface oxide, has a similar EDX signal which hints at $Ni_3Si$ whose stoichiometry is indistinguishable from the main

phase. We thus observe 7 nm of $Ni_3Si$ and 10.2 nm of $Ni_{31}Si_{12}$ with a few nm thick mixing zone of Si(Ni), matching the estimations based on the sheet resistance.
For 400 °C similarly, two phases are distinguishable by TEM which can directly be determined as $Ni_2Si$ and NiSi by the obtained Ni- and Si-EDX signals. We thus obtain 8 nm of $Ni_2Si$ on the top and the main layer of 14.8 nm of NiSi with a Si(Ni) mixing layer of a few nm. The observed phase composition is again in good agreement with the expectations based on the electrical characterization, validating our estimative model.

In consequence, the measured sheet resistances for the bulk samples allow a realistic estimation of the present phases and their thickness ratio. Furthermore, the here presented results already highlight the difference in obtainable phases depending on the used annealing technique. Silicides formed by low-temperature RTA exhibit nickel-rich phases such as $Ni_3Si$ and $Ni_{31}Si_{12}$ though high-temperature intermediate phases such as $Ni_3Si_2$ were not observed by either TEM or electrical characterization for any tested annealing condition. The new Ni-Si phase sequence as obtained by RTA is presented in **Figure 12**.

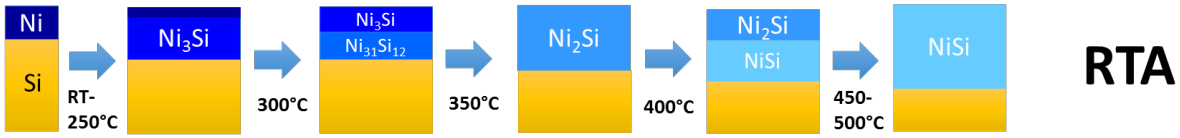



**Figure 12: Schematic representation of the phase evolutions during silicidation of the Ni-silicide system as prepared by rapid thermal annealing (RTA) of Ni thin films. The obtained phases at low temperatures differ from the observable phases obtained by conventional furnace annealing (CFA) as shown in Figure 1.**

# 3 Contact silicidation on vertical Si-nanowires using Ni and NiPt

In this chapter, results on the silicide contact fabrication on vertical silicon nanostructures are presented. The focus on the investigation thereby lies on the impact of the different geometrical constraints of such nanowires and their respective sizes (diameter) on the silicidation process. Nanostructure fabrication is detailed in **Section 3.1** while the metal deposition and contact annealing by RTA follows the same procedure as described in **Section 2.1**. The prepared 3D-silcide structures are finally characterized in detail through transmission electron microscopy (TEM) and energy dispersive X-ray analysis (EDX) performed in a JEOL JEM-ARM200F microscope as presented in **Sections 3.2 and 3.3** for nickel and nickel-platinum alloys.

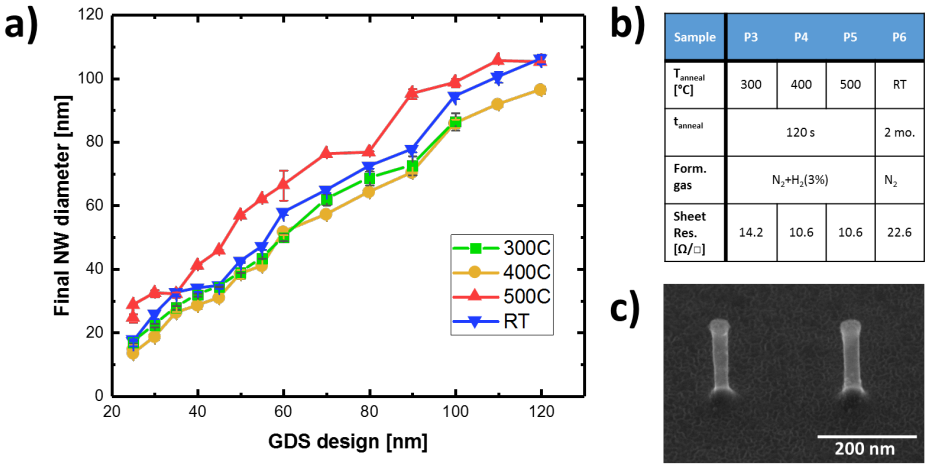
## 3.1 Nanowire fabrication and silicide sample preparation

Differently sized nanowires (NW) have been fabricated by a top-down approach on p-type silicon (Boron-doped at $1\text{-}2\cdot10^{19}$ $cm^{-3}$). The patterns were defined by e-beam lithography (EBL) using a high-resolution negative-tone resist, namely Hydrogen SylesQuioxane (HSQ), in a Raith-150 system at minimal spot size and an acceleration voltage of 30 kV. After development in 25% Tetramethylammonium hydroxide (TMAH) and rinse in Methanol, the resulting structures are highly vertical. These nano-patterns were then transferred onto the substrate by an inductively coupled plasma etching (ICP-RIE) in an Alcatel AMS4200 system. The fluorine-based reactive ion etching (RIE) is perfectly anisotropic and has been used to create structures of 200-220 nm height. Any remaining HSQ was removed after submersion in diluted hydrofluoric acid, followed by a low-power oxygen plasma cleaning (20 W for 30 s) to remove any carbon residues introduced in the primary plasma etching process. The nanostructures' dimensions were further reduced through the creation of a sacrificial oxide layer and its

successive removal in a buffered oxide etchant (BOE) solution. The oxide thickness could be adjusted to thin or thick layers using dry or wet-thermal oxidation processes in a Centronic E1550HT tube furnace.
Before the metal deposition, following the general description provided in **Section 2.1**, any native oxide on the prepared nanostructures was removed by dipping in diluted hydrofluoric acid. The silicidation process was successively activated by rapid thermal annealing (RTA) in an AS-One rapid-thermal processing furnace. Samples were heated up to 300-500 °C for 2 minutes under a 3% $H_2/N_2$ atmosphere. The nanostructures were observed during the different process steps by scanning electron microscopy (SEM) and finally prepared for TEM observation by a focused ion beam (FIB) in an FEI Helios 600i double beam system. For the fabrication of the TEM lamella, a carbon-contrast layer of 50 nm was deposited on the structures followed by a protective Pt layer of more than 500 nm.

## 3.2 Nickel silicide on Si nanostructures

Three samples including large arrays of NWs with sizes of 20-100 nm in diameter and an initial nickel deposition of 12 nm were annealed for 2 minutes at 300, 400, and 500 °C in order to assure the formation of NiSi. A fourth sample, without an annealing process, serves as a reference. The NW sizes, fabrication details, and measured sheet resistance of the bulk layers are presented in **Figure 13**.




| Sample | P3 | P4 | P5 | P6 |
|---|---|---|---|---|
| $T_{anneal}$ [°C] | 300 | 400 | 500 | RT |
| $t_{anneal}$ | 120 s | | | 2 mo. |
| Form. gas | $N_2$+$H_2$(3%) | | | $N_2$ |
| Sheet Res. [Ω/□] | 14.2 | 10.6 | 10.6 | 22.6 |

**Figure 13: Measurement results of the nanowire diameter of the fabricated nano-structured silicide contacts (a) and thermal processing information including the sheet resistance measurement of the bulk silicide layer surrounding the nanowire structures (b). An exemplary SEM image of prepared nanowires with Ni-Si top contacts is presented in (c).**

Investigating the nickel silicidation by TEM, the nanowires demonstrate a significantly different Ni-Si growth as compared to the bulk. Not only appears the Ni diffusion, and thus the silicide penetration into the nanowire, to be strongly enhanced, but the forefront of the Ni-diffusion is accompanied by a faceted growth (see **Figure 14a**). The facet formation and penetration depth has been measured and is presented in **Figure 14b**. The facet penetration depth not only scales with the temperature but also with the reducing nanowire diameter. It increases linearly once a certain critical threshold diameter is reached. In the case of 300 and 400 °C, the on-set of the linear regime appears at 80 and 60 nm respectively. For silicides formed at high temperature (500 °C), the growth appears to have “leveled out” without any observable size dependence.

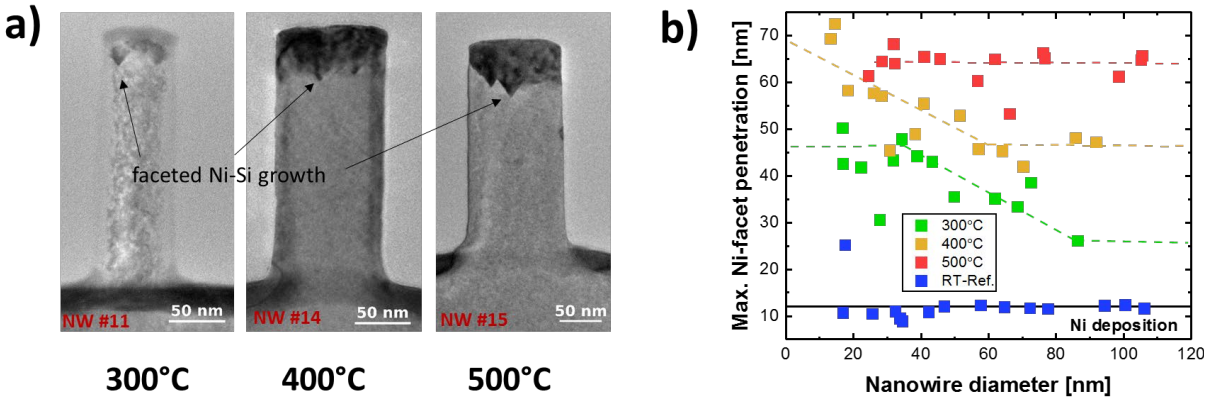



**Figure 14: TEM cross-sections of large Si nanowires with Ni-Si contacts annealed at 300, 400, and 500 °C by RTA. All three nanowires display the main contact layer and a faceted growth of thin Ni-Si phases protruding as triangles into the nanowire (a). The penetration depth of this faceted growth has been measured across the three temperatures for varying nanowire diameters as presented in (b).**

The faceted $Ni_xSi_{1-x}$ phase in all NWs forms edges with angles of 51-55° to the sidewalls, corresponding to the (111) planes of silicon. Such growth has already been reported in the literature for different systems under different conditions. For example, pyramidal structures of epitaxial $NiSi_2$ were observed for ultra-thin films [31] or thin films with oxide interlayer [32] which transform into NiSi beyond 400 °C using CFA. However, for RTA such $NiSi_2$ facets have been observed at higher temperatures of 450 °C in bulk and nanowire structures [33, 34]. On the contrary, Hou et al. have recently demonstrated the appearance of pyramidal structures of $Ni_2Si$ [35] transforming into NiSi during in-situ annealing. While these results are either based on bulk samples or nanowires with a large metal reservoir, Hsu et al. focused on nanowires silicidation using a thick Ni deposition on top of the nanowires as is also the case for the samples presented here. Results from [36] using RTA at 500 °C for 4 min found similar $NiSi_2$ facet growth but only for larger NW diameters, with d >100 nm and smaller NWs exhibiting NiSi instead.
It is thus not possible to identify the observed faceted growth based on previous experiments in the literature.

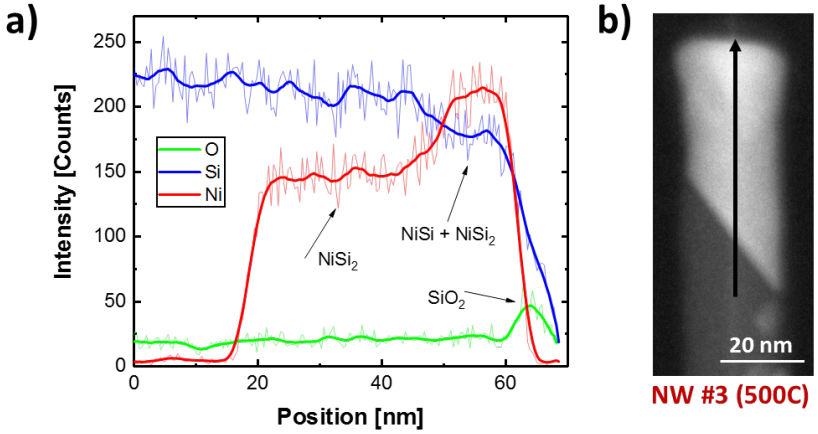



**Figure 15: EDX characterization of the Ni-silicide contact of thin nanowires (ca. 30 nm) after silicidation by RTA at 500 °C for 2 min. The EDX signal presented in (a) has been recorded across the contact as indicated by the black arrow in the STEM image shown in (b). The silicide appears to have been almost completely transformed into NiSi2 while a small amount of NiSi is still retained near the surface. The surface of the contact as well as all around the nanowire is covered in a thin $SiO_2$ oxide layer which has naturally formed after silicidation.**

While it is possible to characterize the main Ni-Si phase atop (the first 10-15 nm) the contact by EDX, the composition of the facets cannot be determined directly because the facets

themselves appear to be thinner than the prepared TEM lamella (thus <<100 nm) and also the total width of most NWs (< 20 nm). Any EDX measurement of the facets has a strongly superposed signal coming from the surrounding silicon. However, for the smallest NWs at 500 °C annealing temperature, the faceted growth appears to fill out the entire diameter of the nanowire, allowing the detection of the facets phase composition revealed as $NiSi_2$ in **Figure 15**. As this faceted $NiSi_2$ growth appears to be consistent throughout all observed nanowires, we hence assume $NiSi_2$ as the phase for all observed facets.
The main NW-silicide layers are also characterized by EDX revealing $Ni_2Si$ and NiSi as the main phases for NWs samples annealed at 300 and 400 °C. For the smallest NW diameters at 300 °C, remnants of $Ni_3Si$ on the contact surface have been found. At 500 °C the entire silicide contact appears to have transformed into $NiSi_2$ though the smallest NWs again retain traces of Ni-rich phases. The obtained results for differently sized NWs are presented in the TEM images of **Figure 16**.

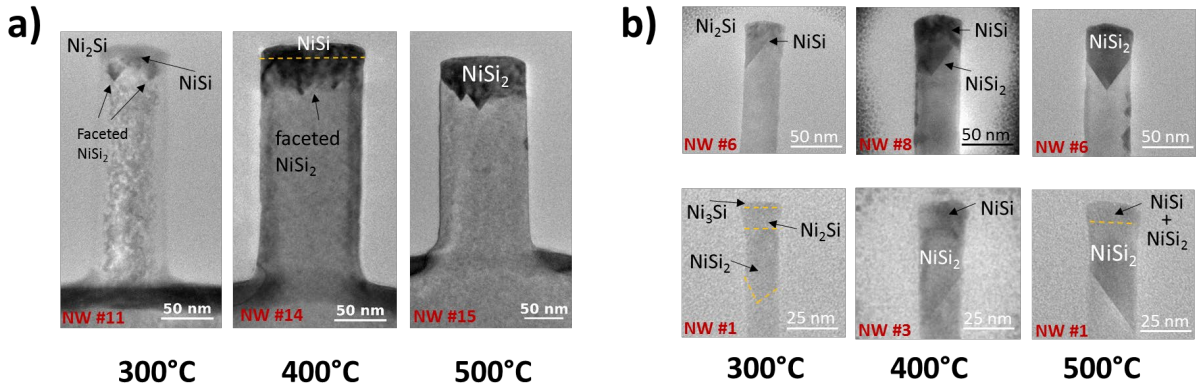



**Figure 16: Comparison of the Ni-Si phase composition by TEM observation of differently sized nanowires after silicidation processes at 300, 400, and 500 °C for 2 min. The phase compositions as determined by EDX have been marked on large nanowires (ca. 100 nm, as shown in Figure 14a) in (a) as well as for medium (45-50 nm) and small NWs (20-30 nm) as presented in (b). While large and medium NWs display the same Ni-Si phases, the overall penetration of the silicide is enhanced. For the smallest NWs thin Ni-rich phases remain on top of the contact.**

In summary, the Ni-Si silicidation in the temperature range of 300-500 °C has been investigated demonstrating a change in the Ni-Si phase transformation imposed by the geometrical constraints of the nanowires. While the main silicide phases are in agreement with the expectations from bulk silicide characterization, for all observed nanowires with diameters of <120 nm, the growth of $NiSi_2$ facets at the contact interface has been observed. The growth and penetration of these facets increase with the silicidation temperature and are further enhanced for reduced NW diameters below a critical threshold depending on the annealing condition. In extension, the complete transformation into $NiSi_2$, driven by $NiSi_2$ facet formation, is shifted to a lower temperature of 500 °C as compared to the bulk transformation which occurs at around 750 °C [13, 14].
As a result, it can be concluded that, for the fabrication of electrical contacts for NW-transistors, the $NiSi_2$-driven phase growth needs to be better controlled or suppressed in order to be able to tune the Ni-Si contact length as well as to minimize the contact resistance.

## 3.3 Impact of Pt alloy in nickel silicide

A commonly applied approach for the suppression of the $NiSi_2$ in bulk contacts, as presented in **Section 1.2** and shown in **Section 2.3.1** for our annealing setup, is the addition of Pt in the Ni-Si contact. Hence a first demonstration of the nanostructured NiPt-contact silicidation has been prepared. 10 nm of NiPt was deposited on identical NW arrays as used in the previous

section and annealed at 400 °C for 2 min. As the sputtering deposition of NiPt is likely to cover the sidewall of the nanowire, the sidewalls have been protected with a thin $SiO_2$ layer of 2-4 nm as grown by dry thermal oxidation at 725 °C for 20 min that was removed from the top of the nanowire by plasma etching. After the salicidation, the remaining metal is removed by wet-chemical etching in a diluted mixture of $H_2SO_4$ and $H_2O_2$ at room temperature for 40 s (etch rate ca. 1 nm/s).
The TEM cross-section of a nanowire with a 35 nm diameter is shown in **Figure 17a**. The metallization on the sidewalls could not be removed and appears to have formed silicide making it resistant to the used wet-etching technique. However, the formation of the NiPt-silicide contact was correctly achieved as the protective oxide layer separated the sidewall material form the contact. A magnified TEM image of the NiPt top contact in **Figure 17b** shows firstly a round head formation which is typically observed for PtSi contacts (e.g. [4]) but furthermore displays a flat and sharp transition at the contact/Si interface. The contact appears to have grown upwards while constricting the NW diameter at the contact to 25 nm.

An EDX investigation of the sample revealed a contamination with gold, stemming from cross-contamination of the used PVD crucible. A clear gold signal was found in a bulk deposition reference (TEM and EDX measurement in **Figure 17c,d**).
The addition of gold and the consequent melting of the Au-Si eutectic phase at 363 °C [37] is responsible for the melting and silicidation of the sidewall metallization. Hence, the expected metal etching is achievable using our fabrication recipe for future gold-free NiPt depositions. As a preliminary result, the observation of alloyed Ni-silicide contacts has demonstrated a well-controlled silicide contact size with a sharp and flat contact interface, free of $NiSi_2$ facets previously observed in pure Ni-silicide contacts.

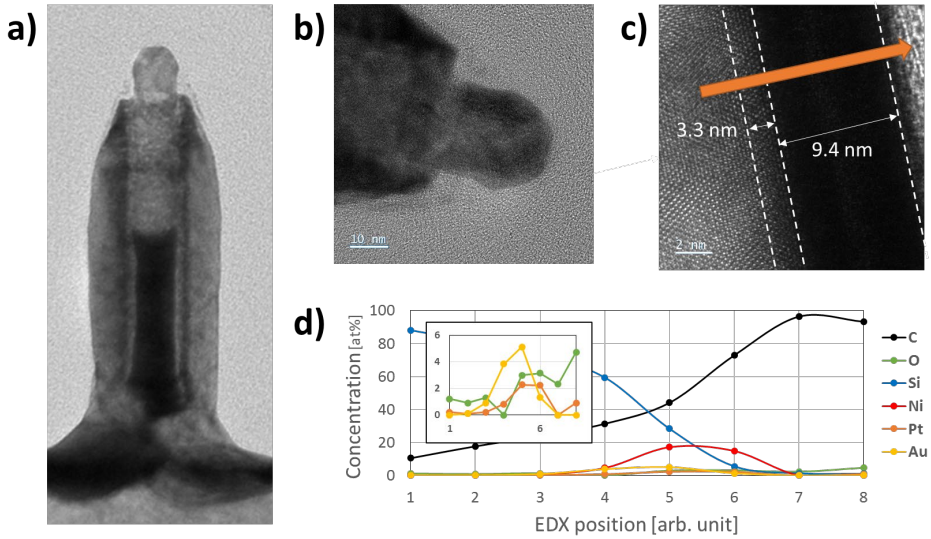



**Figure 17: Cross-sectional TEM observation of a nanowire (a) with silicided NiPt contact, magnified in (b), and remaining metal deposition on the sidewalls. As expected, the addition of Pt in the Ni-silicide contact results in the formation of a well-defined contact with a sharp transition without Ni-rich facets appearing. The sidewall deposition could not be removed by wet-chemical etching and may have partially transformed into silicide due to contamination with gold. Traces of gold at the Si-metal interface were found by investigating the NiPt layer as-deposited shown in (c) by TEM and EDX (d) along the orange arrow.**

# 4 Demonstration of Ni-silicidation on SiGe nanowires

In this chapter, we present a first demonstration of the investigation and fabrication of complex germano-silicide contacts fabricated on nanostructured SiGe substrates (relaxed SiGe substrates are provided by CEA-Leti). Analogous to the Si-system, we first give a brief summary of the known phase transformations found in the literature in **Section 4.1** and electrical characterization of bulk silicides prepared by RTA in **Section 4.2**, before showing the first results on Ni-Ge-Si contacts on SiGe nanowires.

## 4.1 Germanide-silicide formation in the literature

By creating silicide contacts on different substrates such as SiGe alloys one obtains a ternary Ni-SiGe germano-silicidation which differs from the binary silicidation of Ni-Si and Ni-Ge germanidation (see **Appendix 1.3 Figure 22a and Table 5**). While nickel germanide technically forms $Ni_3Ge$, $Ni_2Ge$ $Ni_5Ge_3$, and NiGe (the appearance of $NiGe_2$ only occurs under high pressure), some reports indicate that only a few phases appear. For example, Perrin et al. [38, 39] report on the simultaneous formation of only $Ni_5Ge_3$ and NiGe which is unlike the Ni-Si system where phase formation occurs sequentially, while Yan et al. observed all four phases in nanowire samples [40] (see also [41]). Combining Ni-Ge-Si in a ternary system again changes the observable phases as highlighted by the phase diagram presented in **Appendix 1.3 Figure 22b** with a reduced number of stable phases [42].

As reported in the literature [43], for the thermal process below 350 °C nickel is the dominant diffusing element and forms a quasi-silicide phase $Ni(Si_{1-x}Ge_x)$ at 300-350 °C with the germanium remaining in place. Because germanide phases e.g. NiGe are less stable as compared to NiSi, the Ge is thus integrated into the nickel-silicide. Only for higher temperatures, Ge begins to out-diffuse, decreasing the Ge content in the nickel-germano-silicide to $Ni(Si_{1-y}Ge_y)$ for $y<<x$. Finally, this results in the formation of Ge-free NiSi and Ge-rich phases. In extension, the presence of Ge in the Ni-Si silicide contact has been reported to slow down the formation of high resistive $NiSi_2$, as the associated thermally activated Ge segregation raises the phase transformation temperature, at the draw-back of increased phase/grain boundary agglomeration [44, 45].

## 4.2 Electrical characterization of bulk silicides on Ge-rich substrates

As already presented in **Section 2.3**, bulk samples of Ni-Ge-Si silicides have been prepared by PVD deposition of 9.7 nm of Ni on $Si_{0.5}Ge_{0.5}$ substrates (as-deposited resistivity of 21.4 µΩ cm) and consecutive RTA in the range of 200-600 °C for 2 min using multiple 2·2 $cm^2$ chips. The sheet resistance of those samples has been measured at room temperature with a CMT-SR2000NW 4-probe station and the results are presented in **Figure 18**.

The results show a low resistivity plateau from 400-500 °C corresponding to the mono-silicide phase NiSi(Ge). At 500 °C a strong agglomeration is visible at the surface which leads to a much larger increase in sheet resistance as observed for the formation of $NiSi_2$ in the Ni-Si system. We suspect a simultaneous formation of $NiSi_2$ and Ge-rich phases here. For lower temperatures (<400 °C) the evolution of the sheet resistance is similar to that of the Ni-Si system.

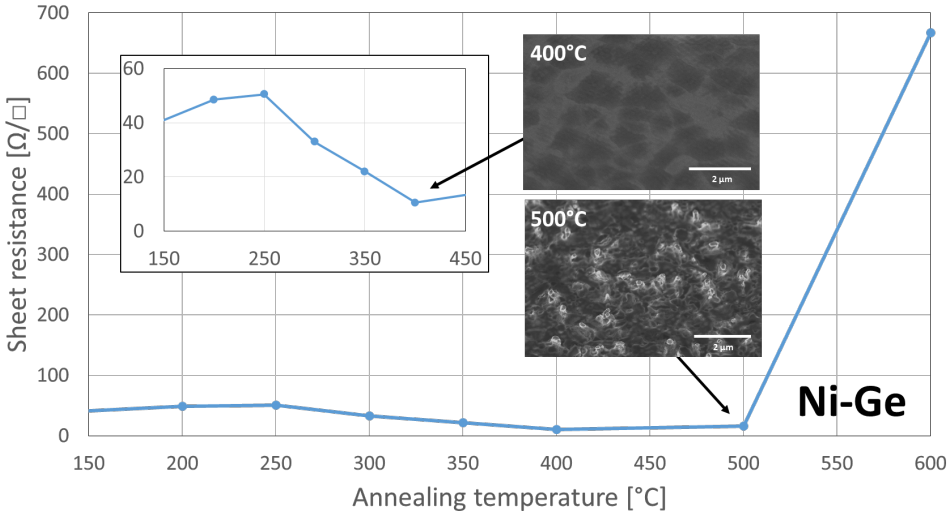



**Figure 18: Sheet resistance of bulk nickel-germano-silicide measured by a 4-point probe. Initial deposition of 9.7 nm of Ni on 2*2 cm$^2$ $Si_{0.5}Ge_{0.5}$ substrates has been silicidied by rapid thermal annealing at different temperatures in the range of 200-800 ˚C for 2 min.**

We conclude that the general appearance of the sheet resistance curve resembles that of the Ni-Si system, indicating a nickel phase dominated silicidation reaction. In effect, the presence of the Ge in the system inhibits the NiSi transformation which has already been observed on $Si_{0.8}Ge_{0.2}$ by Lauwers et al. [46]. The low resistance plateau is thus shortened, starting at a higher temperature of 400 °C while also being cut-off at 500-600 °C due to an earlier transformation of $NiSi_2$ accompanied by a much stronger agglomeration due to expected Ge segregation. These observations are in good agreement with measurements made on pure germanium substrate by Q. Zhang et al. [47].

## 4.3 First demonstration of SiGe nanostructure contact silicidation

Using the same general fabrication process as described in **Section 3.1**, nanowires with varying diameters were fabricated by a top-down approach on a $Si_{0.5}Ge_{0.5}$ substrate. The e-beam lithography as well as the fluorine-based transfer etching have been optimized as presented in deliverable **D4.6** to obtain perfectly vertical nanowires of 200-220 nm height. The remaining fabrication process has been left unchanged, but no sacrificial oxidation was used. Two nanowire samples with an initial Ni deposition of 9.7 nm were annealed at 300 and 500 °C for 2 min by RTA. The formed silicide contacts were observed by TEM and EDX as shown in **Figure 19a-d**.

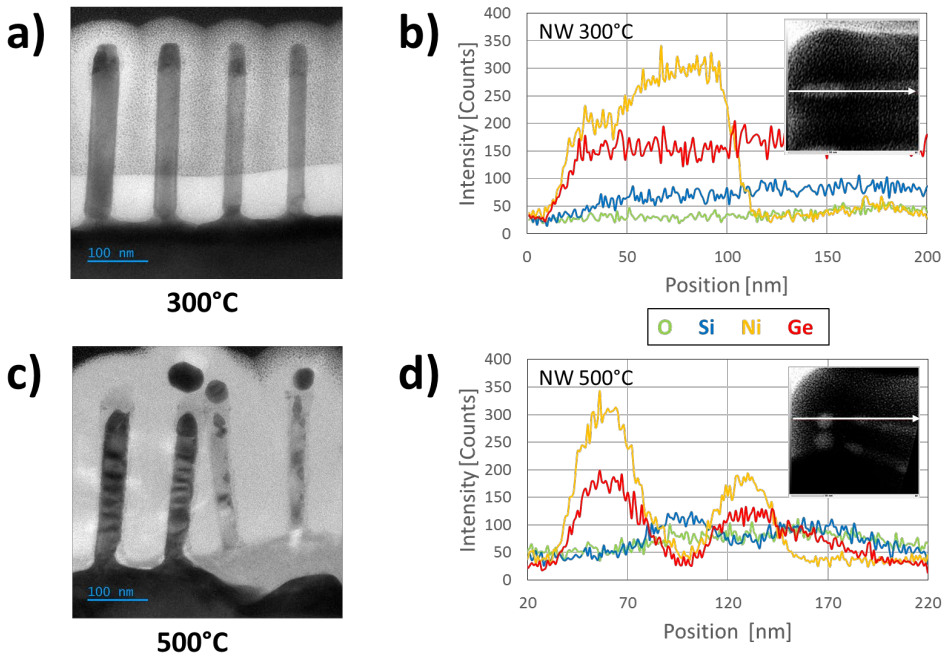



**Figure 19: TEM and EDX characterization of nickel-germano-silicide contacts as fabricated on $Si_{0.5}Ge_{0.5}$ nanowires. The contacts were processed by rapid thermal annealing at 300 and 500 °C for 2 min. As shown in a) the TEM images reveal a well-dimensioned silicide contact with a sharp interface for contacts annealed at 300 °C. Higher annealing temperatures above 500°C result in extensive upward growth of the nanowire contact, separating into multiple phases with recrystallization occurring on top (c). The composition of these Si-Ge-Ni contacts was characterized by EDX as presented in (b) and (d) for 300 and 500 °C respectively.**

At a low annealing temperature of 300 °C, the contact-SiGe interface has a sharp transition but the contacts appear elongated, as compared to the Ni-Si system with a similar metal thickness, measuring 55 ± 5 nm in total thickness across all observed nanowire sizes. The contact is further split into two distinct layers visible in **Figure 19a** and measured by EDX in **Figure 19b**. While the main layer of the contact of ca. 40 nm comprises a Ni-rich alloy with SiGe of the same composition as the nanowire, a 15 nm thin top layer of silicon-free Ni-Ge is formed.

This initial stage of germanide segregation is enhanced for the observed NW after annealing at 500 °C as shown in **Figure19c**. The contact's upwards growth is further increased by splitting into three different layers whose distinct EDX compositions are shown in **Figure19d**. At the bottom interface of the contact, a 20-30 nm thick phase of Ni-Si-Ge remains that should correspond to a NiSi(Ge) mono-sicilicide phase, possibly with a slightly increased Ge concentration as in the bulk NW below. On top, separated by a pure silicon layer, crystalline Ni-Ge phases formed. While the here shown cross-section of a small crystal appears to be Ni-rich, larger crystals as for example shown on the left in **Figure 19c** revealed a 1-to-1 composition of Ni and Ge, indicating a crystalline phase of NiGe as observed in the initial stage at 300 °C.

In summary, we observe the simultaneous formation and/or segregation of NiGe germanide and $Ni_xSi_y(Ge)$ phases in nanowires for lower temperatures than reported in the literature. The initial germanide formation appears to be driven by an upward Ge diffusion while at higher temperature Ge diffusion, Ge segregation, and Ni diffusion clash, creating zoned contacts with NiGe agglomerations crystallizing on top.

To verify the exact process and impact of the Ge diffusion and the initial Ge concentration on the germano-silicidation a more detailed investigation, including also different Ge concentrations, will be required.
For the contact fabrication, it can already be concluded that Ge indeed prevents the formation of $NiSi_2$ but the strong germanide formation and agglomeration for high Ge contents limits the applicability of pure Ni contacts. The addition of Pt, thus implementing NiPt contacts, or other alloy elements that may form a diffusion barrier, regulating the Ge diffusion, would be the next step in the optimization of metal-silicide contacts on SiGe nanostructures.

## Conclusion

In this deliverable, the experimental investigations of the Ni-, Pt- and NiPt-silicidation conducted at CNR-IMM and LAAS-CNRS has been presented. Focusing firstly on the investigation of the early steps of silicide formation in bulk silicide samples as well as the impact of the annealing techniques. Secondly, the impact of geometrical constraints on the silicide phase transformation as observed for silicide contacts fabricated on highly vertical nanowires has been demonstrated with the additional aim to optimize the nanostructured contact fabrication of low resistive NiSi with respect to silicidation processes using a low thermal budget.

In situ characterization of Ni-silicide through XRD and XRR revealed that intermixing occurs already after metal deposition due to adsorption-diffusion-injection mechanisms as observed experimentally by a few nm thick Ni-Si mixing zone with a ratio of 3:1.
The comparison of the Ni and Pt silicidation reactions using the same reaction protocol, using conventional furnace annealing techniques, demonstrated that silicidation is a slower process for Pt than for Ni. It is thus concluded that the initial mixing after deposition of nickel may be the driving force promoting silicidation. The control of the early stage of mixing may thus be applied to tune the structural properties of the reacted silicide layer.
Similar silicide samples using Pt, Ni, and NiPt (10% Pt) were processed by rapid thermal annealing and characterized by 4-probe measurements. It has additionally been verified by TEM observations that the measured sheet resistances of bulk Ni-Si samples allow the accurate estimation of the silicide phases and their comparison to the reported resistivities of Ni-Si phases in the literature. The difference in obtainable phases depending on the used annealing technique has been presented: Silicides formed by low-temperature RTA exhibit nickel-rich phases such as $Ni_3Si$ and $Ni_{31}Si_{12}$ that are commonly not observed for conventional annealing methods.

Using the same rapid thermal annealing process Ni-silicide contacts were fabricated on vertical silicon nanowires. The impact of the geometrical constraints on the Ni-Si transformation was investigated in the temperature range of 300-500 °C. All observed nanowires (diameter <120 nm) showed faceted growth of $NiSi_2$ at the contact interface whose penetration depth increased with the silicidation temperature and reduction in NW diameter. In consequence, the full transformation of $NiSi_2$ NW contacts appears at a lower temperature than for the bulk system. In order to suppress the growth of $NiSi_2$, Pt can be added to the contact as was demonstrated for bulk samples using an initial deposition of 10 nm thick NiPt. The first results on fabricated NiPt nanowire contacts demonstrated a well-controlled silicide contact size with a sharp and flat contact interface, free of $NiSi_2$ facets previously observed in pure Ni-silicide contacts. A detailed investigation of NiPt-silicide NW contacts, especially in regard to the low temperature (300 °C) silicidation of NiSi, is envisaged for the following works.

Lastly, a first demonstration of the Ni-silicidation on Ge-rich $Si_{0.5}Ge_{0.5}$ substrates and nanowires, fabricated using optimized fabrication processes detailed in deliverable **D4.6**, has been provided. While Ge as an alloying element reduces the formation of $NiSi_2$ similar to Pt, it is known to cause strong agglomeration which was observed for bulk and nanowire samples. The simultaneous formation and segregation of NiGe germanide and $Ni_xSi_y(Ge)$ phases, driven by an upward Ge diffusion has been observed. At high temperatures above 500 °C, this leads to zoned contacts with NiGe agglomerations crystallizing on top. For nanowires, the initial stage of NiGe formation is already visible at low temperatures of 300 °C. A more detailed investigation, also including NWs with different Ge-concentrations, will be required to understand the reaction mechanism. While Ni-silicide on SiGe does not form $NiSi_2$, the strong germanide agglomeration needs to be controlled for future device applications. The effectiveness of alloys such as Pt, with Pt potentially providing a diffusion barrier, for the prevention of NiGe formation/segregation has to be tested.

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# Appendix

## Appendix 1.1 Pt-Si phase diagram

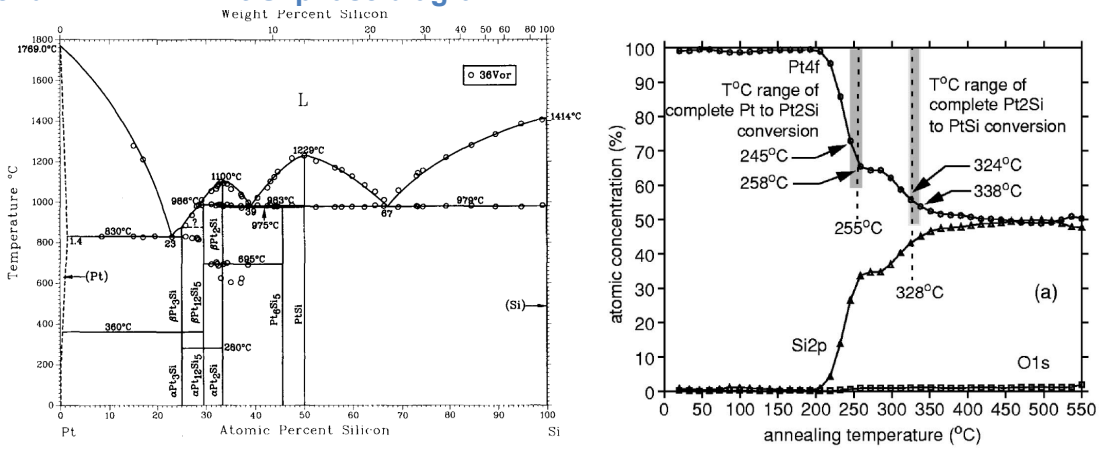


**Figure 20: Full Pt-Si phase diagram for high temperatures (a) [9] and observed Pt-Si transformation for bulk contact annealing by RTA [6].**

**Table 3: List of the 6 important Pt-Si phases to be formed after low-temperature annealing processes taken from [8] and [6, 48, 49]. * NW values form [30]**

| Phase | Density [g/cm$^3$] | Resistivity range [μΩ cm] | T formation [°C] | Silicide ratio [t/t] | Si consumption [t/t] |
|---|---|---|---|---|---|
| Pt | 21.4 | 10.6 | - | - | - |
| $Pt_3Si$ | 16.72 | 76-250 | 125-350 | ? | ? |
| $Pt_{12}Si_5$ | 16.01 | 67-167 | ? | ? | ? |
| $Pt_2Si$ | 14.62 | 41-100, 6.5* | 200-330 | 1.43 | 0.66 |
| $Pt_6Si_5$ | 12.65 | 41-71 | ? | ? | ? |
| PtSi | 12.4 | 52-250, 28* | 320-700 | 1.97 | 1.32 |

## Appendix 1.2 Ni-Si phase diagram

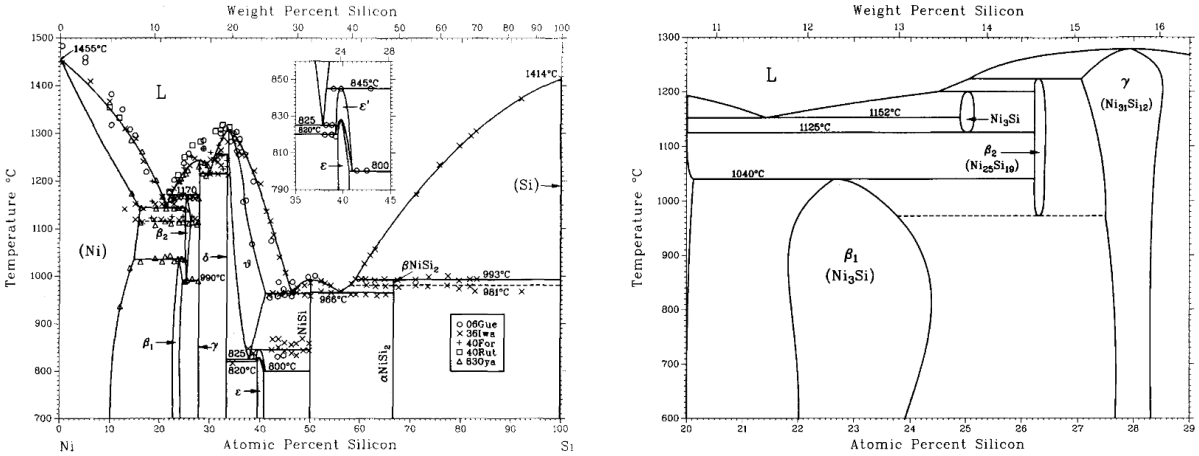


**Figure 21: Full Ni-Si phase diagram for high temperatures (a) and an enlarged section for nickel-rich mixtures (b) as taken from [12].**

**Table 4: List of the seven important Ni-Si phases to be formed after low-temperature annealing processes taken from [19, 22] with resistivity measurements taken from [19, 50-54]. Single resistivity values from various literature publications have been selected as a primary reference. *The listed $Ni_3Si_2$ phase is also referred to as delta-$Ni_2Si$ in other literature (see e.g. [55]).**

| Phase | Density [g/cm³] | Resistivity range [μΩ·cm] | Single Res. [μΩ·cm] | Silicide ratio [t/t] | Si consumed [t/t] |
|---|---|---|---|---|---|
| Ni | 8.91 | 7-10 | 6.9 | 1 | 0 |
| $Ni_3Si$ | 7.78 | 80-90 | 72 | 1.31 | 0.61 |
| $Ni_{31}Si_{12}$ | 7.56 | 90-150 | 90 | 1.40 | 0.71 |
| $Ni_2Si$ | 7.51 | 24-30 | 24 | 1.47 | 0.91 |
| $Ni_3Si_2$ * | 6.71 | 60-70 | 60 | 1.75 | 1.22 |
| NiSi | 5.97 | (10.5) 14-18 | 10.5 | 2.20 | 1.83 |
| $NiSi_2$ | 4.80 | 34-50 | 34 | 3.61 | 3.66 |

## Appendix 1.3 Ni-Ge and Ni-Ge-Si phase diagrams

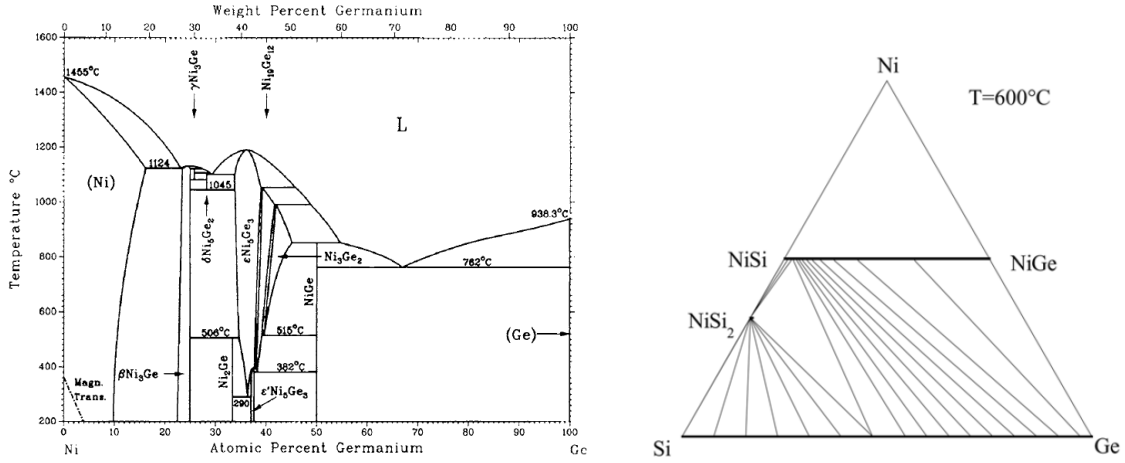


**Figure 22: Binary phase diagram of Ni-Ge as taken from [56] (left) and the ternary phase diagram for the Ni-Si-Ge system as calculated for a temperature of 600 °C [42] (right).**

**Table 5: List of stable Ni-Ge phases as reported in [57-59]. The $Ni_2Ge$ may be metastable and is known to decompose into $Ni_3Ge$ and $Ni_5Ge_3$. * Only formed under high pressure (5 GPa); *1 Measured on nanowires [60]; *2 measured on thin films [61, 62]; *3 measured on nanowires [40].**

| Phase | Density [g/cm³] | Resistivity range [μΩ cm] | T formation [°C] | Silicide ratio [t/t] | Si consumed [t/t] |
|---|---|---|---|---|---|
| Ge | 5.323 | $10e^3$-$10e^8$ | - | - | ? |
| $Ni_3Ge$ | 9.01 | ? | <250 | ? | ? |
| $Ni_2Ge$ | 8.90 | 23 / 88 *1 | 250 | 1.57 | ? |
| $Ni_5Ge_3$ | 8.58 | 132 *3 | 250-300 | ? | ? |
| NiGe | 7.99 | 16-18, 17-24 *2, 35 *3 | 300-450 | 1.18 | ? |
| $NiGe_2$ | ? | 70 | 700* | 1.99 | ? |

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