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Modeling Unconventional Nanoscaled Device FABrication

D5.1: First batch of experimental results regarding the electrical and structural characterization of device samples

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Contents

Abstract

This deliverable reports on the first batch of experimental characterization results of devices within work package 5. The first part deals with the structural characterization of the silicon/dielectric interface of an atomic layer deposition (ALD) high-k gate stack using transmission electron microscopy (TEM) and energy-dispersive X-ray (EDX) measurements. The second part of the deliverable is concerned with the electrical characterization of high-k devices provided by CEA-LETI in order to experimentally extract parameter distributions of electrically active border traps. A novel extraction technique is used to infer physically reasonable defect distributions from the obtained measurement results.

1 Device Characterization

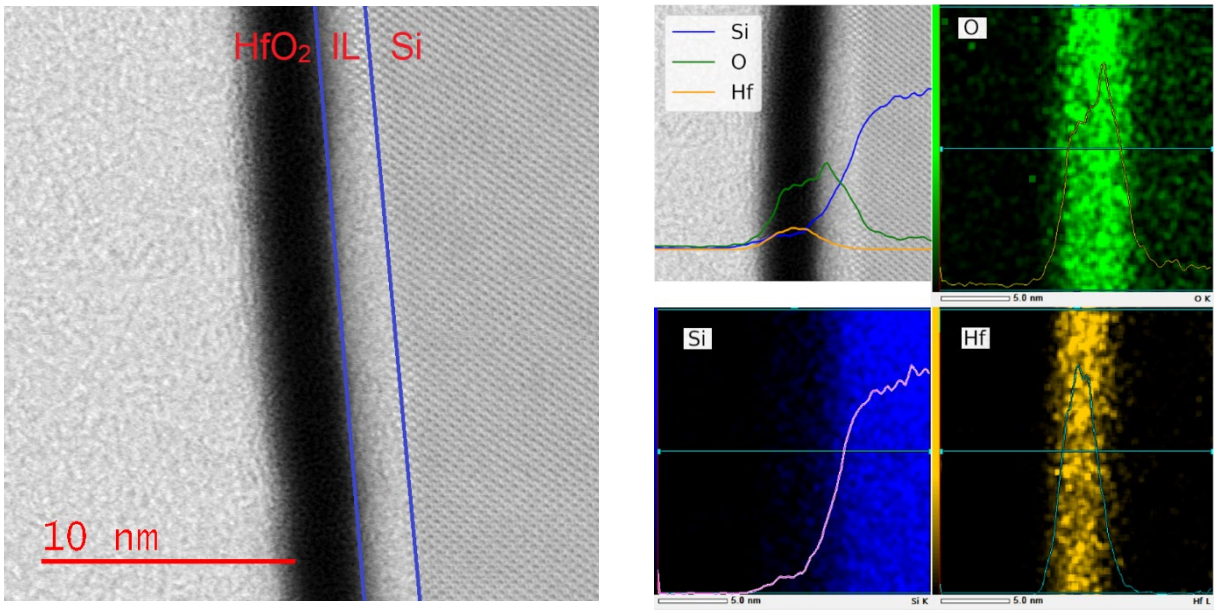

*Figure 1: TEM image of the device after 27 cycles of ALD deposition **(left)**. The interfacial layer (IL) forming between HfO_2 and Si is clearly visible with a thickness of approximately 1.7nm. EDX measurements showing the distribution of Hf (yellow), Si (blue) and O (green) within the structure **(right)**. According to the EDX signals, the IL mostly consists of SiO_x, with Hf only occurring close to the HfO_2 interface.*

1.1 Structural Characterization

For the structural device characterization within Task 5.4, devices with a high-k gate stack were fabricated at CEA using an atomic layer deposition (ALD) process for the deposition of hafnia (HfO_2) on a HF cleaned Si substrate. The HfO_2 deposition was done at 250°C from a mixture of the precursor *Tetrakis-(dimethylamino)-hafnium(IV)* (TDMAH) and moisture (H_2O). In total, 27 ALD cycles were performed, resulting in a nominal layer thickness of 3.8nm. The obtained device structures were subsequently analyzed by transmission electron microscopy (TEM). As shown in Fig. 1 (left), the devices exhibit a high-quality uniform interface. The samples show a rather thick interfacial layer (IL, approx. 1.7nm) compared to usually reported 0.5nm when using the more common $HfCl_4$ precursor [1]. However, the thick IL observed in our samples is consistent with other studies using TDMAH as a precursor, see e.g. [2]. In order to investigate the structural device properties further, energy-dispersive X-ray (EDX) spectroscopy was conducted. The resulting distributions of Hf, Si and O across the interface are depicted in Fig. 1 (right). As can be seen, Hf is only present in the IL up to a

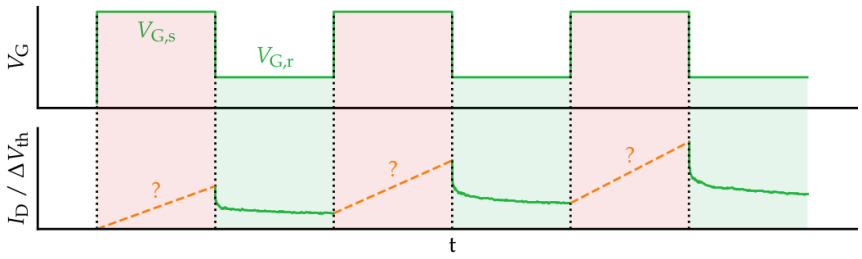

Figure 2: Schematic V_G and $I_D/\Delta V_{th}$ during an extended measure-stress-measure (eMSM) sequence. The device is repeatedly stressed at $V_{G,s}$ followed by a recovery phase at $V_{G,r}$ in which the ΔV_{th} is recorded. Note that during the stress phase, no ΔV_{th} is measured. Reprinted from [15].

depth of about 0.3nm from the HfO_2 interface, hence the IL is mostly comprised of SiO_x with varying stoichiometry between the Si and HfO_2 interface.

1.2 Electrical Characterization

Electrical characterization of devices is one of the main tools in semiconductor industry to determine the quality and reliability of MOSFET devices during operation. The most common techniques for electrical characterization of the time-zero device variability include capacitance/voltage and Id(Vg) measurements, which allow for the extraction of the device electrostatics as well as the charging dynamics of fast interfacial traps. However, in order to extrapolate the reliability over the device lifetime at typical operating conditions, the degradation of the device has to be accelerated by applying high gate voltages at elevated temperatures. Under these stress conditions, the device degradation can be observed within a reasonable time frame (typically hours to days). By calibrating a physics-based reliability model to the accelerated degradation, one obtains a viable framework from which the degradation during operation can be extrapolated. All electrical measurements reported here have been gathered with an in-house custom-built low-noise measurement equipment developed at TU Wien [3]. The devices used for electrical characterization are fully-depleted silicon-on-insulator (FDSOI) CMOS devices provided by CEA-LETI as part of Task 5.4. The devices have a 7nm monocrystalline silicon layer on top of a 145nm thick buried oxide (BOX). The gate stack consists of a chemical oxide interlayer with a thickness of approximately 0.5nm with a 2nm HfO_2 high-k layer deposited on top, followed by a 6.5nm TiN gate. A low-temperature CVD process with a thermal budget of 500°C is used. Further details on the process are given in [1].

Bias Temperature Instability Characterization

Bias temperature instability (BTI) is one of the most prominent reliability concerns in modern scaled MOSFET devices. It is primarily caused by charge trapping at oxide defects, which leads to a change of the electrostatics, measurable as a shift of the threshold voltage (ΔV_{th}). In order to characterize the charge (de)-trapping dynamics of the defects one has to apply a series of gate biases to repeatedly drive the defects out of thermal equilibrium. E.g. in the commonly employed *extended Measure-Stress-Measure* (eMSM) scheme, sequences made up of repeated stress and recovery phases with different stress voltages are applied at different temperatures. An exemplary eMSM sequence used for the test devices and the resulting temporal development of the ΔV_{th} degradation is shown in Fig. 2. Since ΔV_{th} is only indirectly accessible in experiment, an equivalent change in the drain current I_D is recorded with a transimpedance amplifier as shown in Fig. 3 (left). Using the initial $I_{\mathrm{D}}(V_{\mathrm{G}})$ of the device

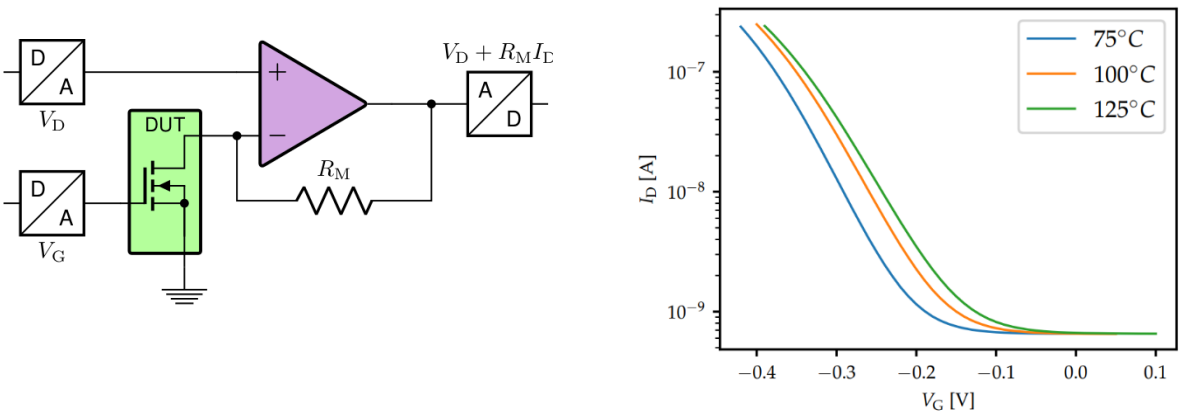

*Figure 3: Schematic circuit for measuring the ΔI_D shift of a device under test (DUT) using an OpAmp based transimpedance amplifier **(left)**, Reprinted from [15].* Measured *I_D-V_G curves for the CEA-LETI devices **(right)** at different temperatures for model calibration.*

before stress, see Fig. 3 (right), the obtained ΔI_D is mapped back to ΔV_{th}. The transfer characteristics are measured at different temperatures in order to allow an accurate calibration of device models which are later used to extract defect parameters like the trap level or relaxation energy from the eMSM experiments.

2 Modeling and Defect Extraction

The following gives a brief description of the physical device modelling necessary to infer physically meaningful defect parameters from experiments. Furthermore, we will address the generally difficult task of parameter estimation with our newly developed automated extraction method [4]. This technique will be used to infer important defect parameters like the trap level or the relaxation energy from accelerated ΔV_{th} measurements at various temperatures and bias conditions. Using a physical device model, these parameters can then be used to predict the device reliability at operating conditions.

2.1 Nonradiative Multiphonon Model

Even though the eMSM experiments provide the macroscopically visible ΔV_{th} degradation, as elaborated in the last section, this information alone is not sufficient to directly predict the degradation at different (e.g. operating) conditions. For this aim, a physically motivated charge trapping model, whose parameters are inferred from the ΔV_{th} degradation, can be used to 1) extrapolate the degradation to arbitrary bias/temperature conditions and 2) gain physical information on electrically active oxide defects. Since the defects strongly couple to the surrounding heat bath and hence can dissipate energy via the emission of multiple phonons, modeling the charge transfer process requires a treatment within nonradiative multiphonon (NMP) theory. Here, the defects are described within a 2-state NMP model [5], where a charged and an uncharged defect state are included, both of which are approximated as harmonic oscillators around their equilibrium atomic configurations. The corresponding potential energy surfaces (PES) relative to the device band diagram are shown in Fig. 4. Typically, the PESs in the model are defined by the thermodynamic trap level E_T, the relaxation energy E_R as well as the curvature ratio R between both surfaces. Furthermore, the distance x_T between trap and device substrate introduces a bias-dependent energy difference between the two defect states. At or above room temperature, usually a classical approximation of the NMP model can be applied [6]. In this description the barrier given by the intersection of the two PESs has to be overcome for a charge transfer to

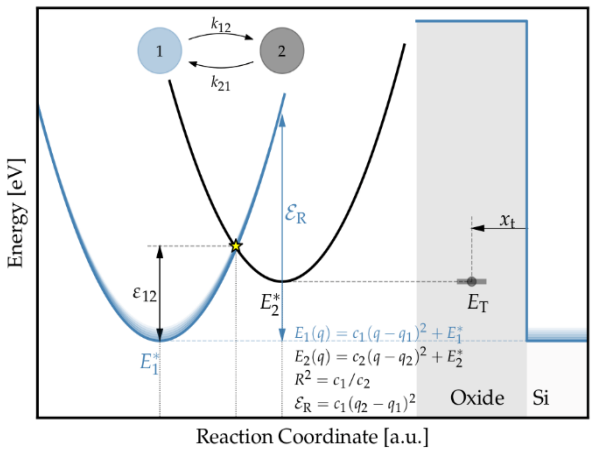

Figure 4: Charge transfer within a two-state nonradiative multiphonon model. The differently charged defect states are treated as one-dimensional harmonic oscillators. The trap level E_T as well as the relaxation energy E_R are important model parameters to identify possible defect candidates. Reprinted from [4].

happen and thus determines the resulting transition rate. Using these approximations, the capture/emission times of a particular defect are fully described by [5]

$$1/\tau_{12} = n v_{th} \vartheta \sigma \, exp(-\varepsilon_{12}/k_B T)$$

with ε_{12} being the classical barrier as a function of the intrinsic defect parameters (E_T, E_R, x_T) as well as the applied bias Vg. The additional prefactors are the concentration of carriers n and their thermal velocity v_{th}, the Wentzel-Kramers-Brillouin (WKB) tunneling factor ϑ and the capture cross section σ. Subsequently, such a degradation model can be calibrated to a particular technology by inferring distributions for the defect parameters based on the available ΔV_{th} measurements, as will be discussed below.

2.2 Effective Single Defect Decomposition (ESiD)

Due to the amorphous nature of the gate dielectric, the environments of defects vary, leading to inherent distributions of defect parameters like E_T, E_R even within the same trap species. Earlier works [7] [8] proceeded by simply assuming a specific analytical distribution function, most commonly Gaussians with a certain mean and variance, and use its parameters like mean and standard deviation as fitting parameters to match the experimental degradation. In this way a defect distribution can be handily described as a “trap band” defined with a handful of simple parameters. For example, in our in-house reliability simulator Comphy [8], a defect band is given by the parameter set

$$(E_T, \sigma_T, E_R, \sigma_R, R, x_T).$$

While this approach has been applied frequently in the past due to its simplicity, we recently demonstrated that strictly relying on pre-defined distribution functions can lead to spurious solutions of the fitting problem [4]. For instance, implicit cross-correlations, most notable between E_R and R, can lead to non-unique and potentially unphysical parameter sets. Since this correlation prohibits the simultaneous experimental extraction of E_R and R, we constrain the model to the linear-electron phonon coupling regime ($R = 1$) [9], which is consistent with ab-initio calculations for various defect candidates in a-SiO_2 [10]. Furthermore, the experimentally observed degradation might only stem from the tails of the chosen distribution

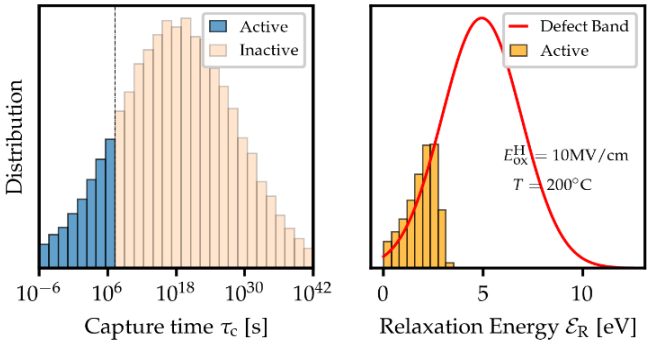

*Figure 5: When strictly assuming a Gaussian parameter distribution **(left)**, the resulting defect bands can show unphysically large time constants **(right)**, since only the distribution tail contains actual electrically active defects. Electron trap parameters for SiON extracted in [8] are used here.*

function, with large portions of the theoretical defect band being entirely inactive within the measurement window due to their large relaxation energies. This case is illustrated in Fig. 5 for electron traps in SiON extracted in an earlier work [8]. Without proper consideration, these peculiarities limit the physical meaning of the obtained defect bands and make identification of potential defect candidates by comparison to theoretical parameters, e.g. obtained from DFT calculations, more challenging.

In order to resolve these issues, we employ our recently developed extraction scheme, named *effective single defect decomposition* (ESiD) [4]. Contrary to other parameter estimation techniques, ESiD does not require a predefined distribution function for the defect parameters, but rather expands the ΔV_{th} degradation in terms of effective single-defect contributions. An exemplary decomposition of negative BTI (NBTI) degradation on a pMOSFET using this technique is shown in Fig. 6. The output of the algorithm is a distribution function for defect parameters reproducing the input measurement data. Since decomposing the total macroscopic degradation is, mathematically speaking, an ill-posed inverse problem, additional constraints on physically acceptable solutions need to be imposed. In the case of ESiD, a Tikhonov-regularization [11] is used to enforce smooth distribution functions yielding the lowest possible total defect concentration still sufficient to reproduce the measurement data. In the following, ESiD will be employed to obtain defect distributions causing NBTI and positive BTI (PBTI) in high-k devices produced with a low thermal budget of 500°C provided by CEA-LETI.

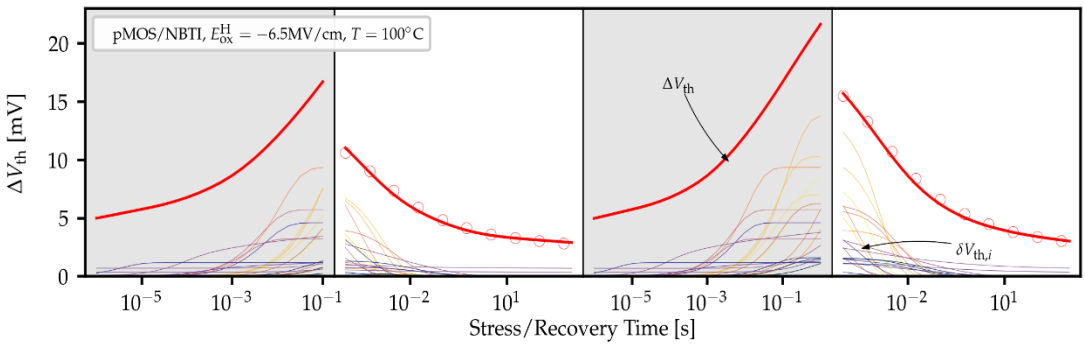

Figure 6: Decomposition of a measured ΔV_{th} trace into effective single defect contributions using ESiD. As can be seen, the different contributions span a large range of timescales as expected from the well-known universal relaxation of BTI observed across multiple technology nodes [12]. The figure is reproduced from [4].

2.3 Results

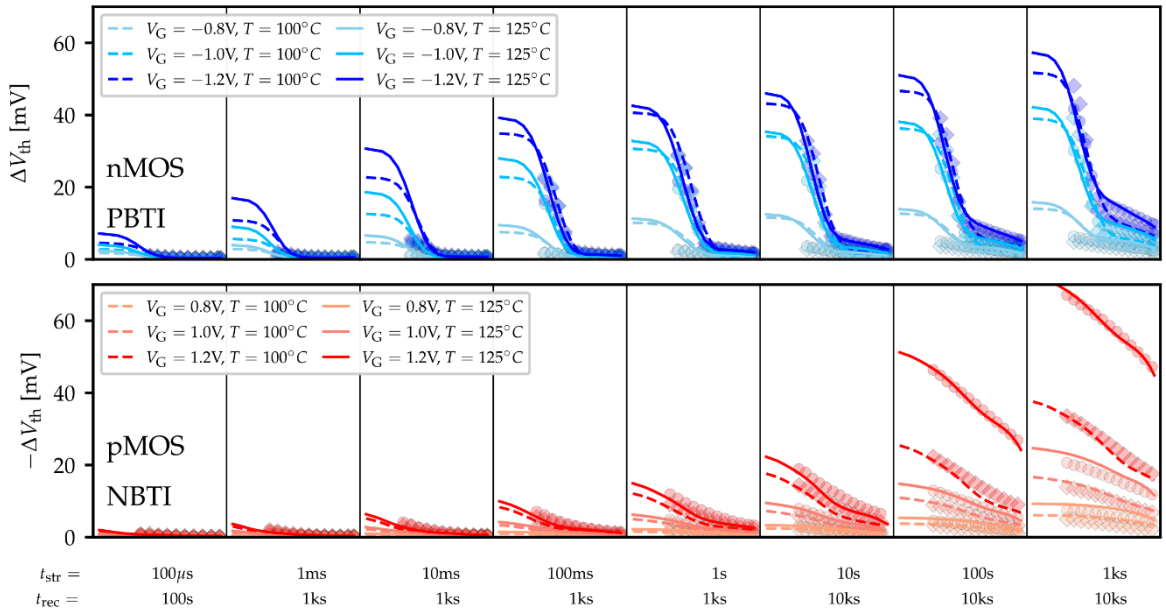

Figure 7: Measured ΔV_{th} (markers) for PBTI and NBTI stress on nMOS and pMOS devices respectively together with the BTI model predictions obtained with ESiD (lines). As can be seen, the model reproduces the experimental data over a wide range of stress and recovery times (100µs to 10ks). Remarkably, the electron traps visible under PBTI conditions can be separated in fast and slow traps. The devices were produced by CEA-LETI.

2.3.1 BTI Model

In order to obtain sensible defect distributions allowing for a robust extrapolation of the device behavior over its lifetime, experimental degradation data has to be provided for various temperatures and gate biases. Here, the devices were subject to NBTI and PBTI stress at temperatures ranging from 75°C to 125°C. Given their industrial relevance, we focused on the combinations NBTI on pMOS and PBTI on nMOS devices, providing a clear separation between hole and electron traps respectively.

The acquired eMSM measurement data was analyzed using our ESiD extraction method. A comparison between the experimental data and the final degradation model created by ESiD is shown in Fig. 7. As can be seen, the automatically developed model accurately reproduces the measured degradation over a wide variety of conditions and over stress times ranging from 100µs up to 1ks. Note that contrary to Fig. 6, only the recovery phase, where measurement data is available, is shown here. In the case of NBTI, the recovery of ΔV_{th} occurs almost uniformly on a logarithmic timescale, reflecting the well-known universal recovery behavior observed in SiON devices more than a decade ago [12]. On the other hand, the electron traps responsible for PBTI split into separate fast and slow defect bands as illustrated in Fig. 7. This finding is consistent with the observation of usually higher noise levels in nMOS devices compared to their pMOS counterparts [13]. While the fast electron band causes a quickly decaying ΔV_{th} response under PBTI conditions, it might be responsible for increased noise at equilibrium operational conditions.

2.3.2 Extracted Defect Bands

While the obtained BTI model demonstrated in the last section provides an accurate description of the macroscopically measurable degradation, due to its physical foundations the internal model parameters also reveal the underlying parameter distributions of physical oxide defects. The obtained defect parameters are shown in Fig. 8. In order to account for the different chemical environments in the interfacial layer (IL) and the bulk oxide (see also Fig.1 left), different defect parameters were allowed in those regions. A summary of the used parameter search regions for the ESiD algorithm as well as the total resulting trap densities are listed in Tab I. The search regions in parameter space are chosen based on typical values obtained in earlier DFT investigations for a-SiO_2 defects. Note that the extracted defect densities using ESiD are roughly 10x lower compared to previous extractions on similar devices [8] using Gaussian distributed parameter sets. As explained earlier in the context of Fig.5, the previously extracted high densities are an artifact of enforcing a particular shape for the distribution functions. For the hole traps in the IL, we observe similar densities and E_T, E_R distributions compared to previously extracted defects in the IL of SiON devices [4]. We attribute this finding to the fact that during the oxide deposition a thin SiO_2 layer is forming as soon as oxygen is involved in the process. We therefore expect the defects located in the IL layer to be similar to defects in bulk a-SiO_2. In particular, the defect parameters for the hydrogen bridge and the hydroxyl-E' center calculated via DFT match our experimental results well. The extracted hole traps in the IL lie approx. 0.8-1.0eV below the Si midgap, in good agreement with earlier investigations [14]. We furthermore observe that the high-k HfO_2 layer introduces a hole trap density 10 times larger compared to the IL layer with a considerably broader distribution of trap levels near the valence band edge of Si. So far the microscopic nature of these traps has not been identified. For PBTI and electron traps on the other hand, we found fairly comparable defect bands in the high-k and the IL layer. The aforementioned separation in fast and slow electron traps is also clearly visible in the resulting distribution of relaxation energies.

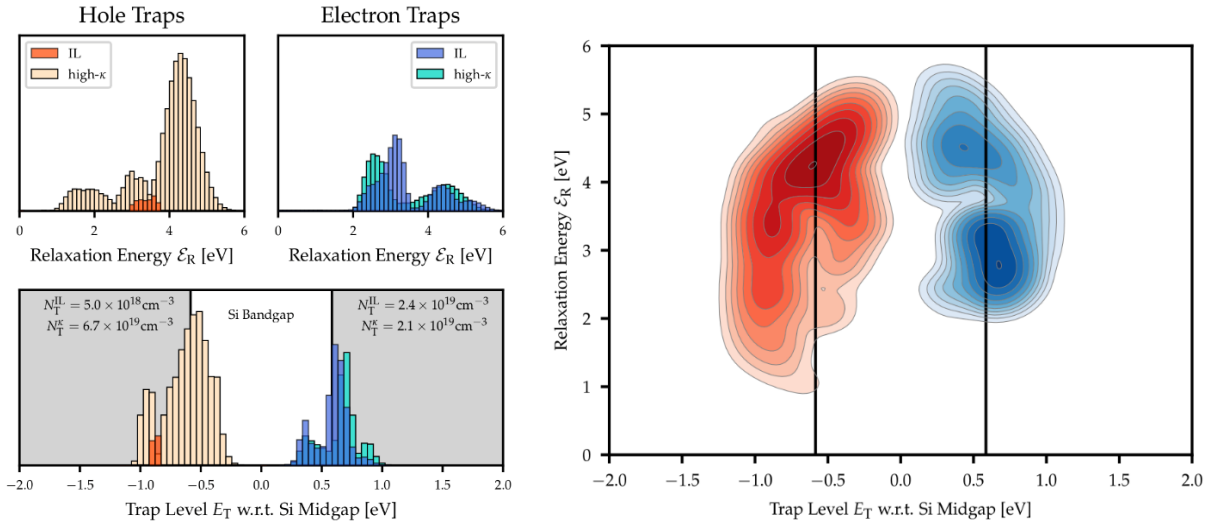

*Figure 8: Defect parameters for each individual defect band represented as histograms **(left)** extracted by ESiD [4] from the experimental data of the studied CEA-LETI devices presented in Fig. 7. Most observed hole and electron traps lie in the vicinity of the Si valence and conduction bands respectively. The distribution of the resulting trap levels and relaxation energies is also shown in a 2D heatmap **(right).** Note that the electron traps (blue) can be separated into a fast and a slow cluster based on their different relaxation energies.*

Defect Bands				
	E_T [eV]	E_R [eV]	x_T [nm]	N_T [cm^{-3}]
Hole traps (IL)	-2.0 – 0.0	0.1 – 6.0	0.0 – 0.5	5.0×10^{18}
Hole traps (oxide)	-2.5 – 0.0	0.1 – 6.0	0.5 – 3.0	6.7×10^{19}
Electron traps (IL)	0.0 – 2.0	0.1 – 6.0	0.0 – 0.5	2.4×10^{18}
Electron traps (oxide)	0.0 – 2.5	0.1 – 6.0	0.5 – 3.0	2.1×10^{18}
Grid spacing	0.05	0.125	0.1	–

Table 1: Grid specifications for the ESiD parameter search together with the extracted total defect density within each individual defect band. The separation into an IL and oxide band allows to distinguish the chemically different environments in the interfacial layer and the bulk oxide. The range for the relaxation energies is chosen based on prior DFT calculations of defects in a-SiO_2 [10].

Conclusions and Outlook

We presented the first batch of experimental results concerning the electrical and structural characterization of low-thermal budget devices as part of work package 5. We verified by TEM and EDX measurements that a clean HfO_2/Si interface can be achieved. Between the HfO_2 and the Si substrate a thin interfacial layer of SiO_x is formed. We further electrically analyzed low thermal-budget FDSOI high-k devices and extracted electron and hole trap parameters for the interfacial layer (IL) and the high-k layer allowing for accurate modeling of the device degradation at arbitrary conditions. We used our newly developed extraction method ESiD (effective single defect decomposition) to infer the defect parameters from the experimental results. The obtained hole traps in the IL are similar to earlier investigations on SiO_2 and SiON devices [4], strongly suggesting bulk-like defects such as the hydroxyl-E' center and the hydrogen bridge in a-SiO_2 as promising defect candidates. We further show that electron traps can be separated into fast and slow traps with distinguishable parameter distributions.

The developed measurement and analysis tools will be employed on different process splits in order to identify the impact of processing parameters on the resulting defect parameters. The characterization of these splits will be presented in deliverable 5.4. Using our open-source modeling approaches, defect parameters for these splits can be extracted and will be included in the TCAD workflow developed within the scope of WP6. This will allow to predict the overall device performance and reliability as a function of the processing conditions. Furthermore, the extracted defect parameters can be used to identify suitable defect candidates from ab-initio calculations in conjunction with the ongoing work presented in deliverable 5.5.

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